

High Performance Two-Channel Audio Codec

Features

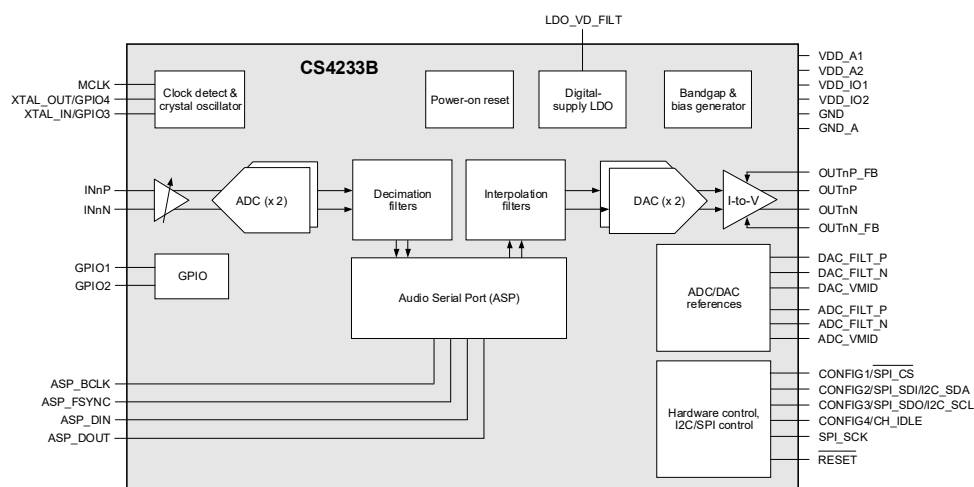
- High performance two-channel codec
 - Differential analog architecture
 - High-resolution 32-bit digital design
 - Low-latency digital filters and digital volume control
- Crystal oscillator interface
- Sample timing alignment across multiple devices
- Virtual passive attenuation device (PAD)
- Clip detection
- Signal-activity detection
- Audio serial port (ASP) sample rates up to 384 kHz
 - I²S, left-justified, and TDM data formats
- Hardware and software control modes
 - I²C control port up to 1 MHz
 - SPI control port up to 24 MHz
 - Hardware control with no host processor required
- Single-supply operation at 3.3 V
 - Support for 1.8 V–3.3 V digital input/output
 - 40-pin QFN package

Specifications

- Advanced multibit sigma-delta ADC
 - 111 dB dynamic range (A-weighted)
 - –107 dB total harmonic distortion + noise (THD+N)
 - 3.9/Fs group delay at 48 kHz sample rate
 - 2 V_{RMS} differential analog input
 - High-pass filter
- Enhanced oversampling sigma-delta voltage-output DAC
 - 110 dB dynamic range (A-weighted)
 - –107 dB total harmonic distortion + noise (THD+N)
 - 4.6/Fs group delay at 48 kHz sample rate
 - 2 V_{RMS} full-scale output

Applications

- A/V receivers
- Digital mixing consoles
- Powered speakers
- Power amplifiers
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments
- Commercial audio systems



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS4233B is a high-performance, 32-bit resolution, two-channel codec. The CS4233B supports differential analog input/output, and 32-bit digital input/output via the audio serial port (ASP) at sample rates up to 384 kHz. The ADC input path incorporates internal analog gain for signal amplification without additional noise or increased power consumption, minimizing external component requirements. Overall system efficiency and performance is enhanced by delivering superior input-referred noise performance and maintaining signal integrity between different applications.

The ADC provides differential architecture, optimized for high performance combined with low power consumption. The CS4233B uses a 5th-order, multibit sigma-delta modulator followed by digital filtering and decimation.

The voltage-output DAC incorporates a proprietary analog FIR architecture to reduce out-of-band noise and minimize the external component requirements. Low-latency digital-interpolation filters are provided. The analog output supports configurable out-of-band filtering, enabling flexible integration and optimal dynamic range for the target application.

The CS4233B can be configured using a control interface supporting I²C™ and SPI™ modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking source, ASP format, and sample rate.

The low-latency digital filters are optimized for the applicable sample rate. A de-emphasis filter is provided in the DAC output path.

The CS4233B includes a virtual PAD function, to emulate a conventional PAD with minimal impact on the noise floor; this minimizes external component requirements leading to a more compact and efficient design. Zero-cross detection is used to synchronize the internal gain changes with zero points in the input signal, avoiding audible gain-change transients. An automatic PAD response feature is incorporated to prevent clipping of large signals at the ASP output.

A signal-activity detection function monitors the input signal on the ADC input paths and DAC output paths to determine signal-activity level relative to configurable thresholds. The signal-activity level status (active or idle) is reported using a dedicated pin that can be monitored by the host to enable a quick and intelligent response to the audio environment, resulting in improved system-level efficiencies and enhanced overall user experience.

The ASP supports operation in I²S, left-justified, and TDM data formats. Tristate control of the data-output pin allows multiple devices to operate on a shared bus.

Clocking for the CS4233B is provided by a separate clock source (MCLK) or else from the crystal oscillator. The ADC-sample and DAC-conversion timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS4233B can be powered from a single 3.3 V supply. Digital input/output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS4233B is available in a commercial-grade 0.4 mm pitch, 40-pin QFN package for operation from –40 °C to +85 °C.

See [Section 11](#) for ordering information.

Table of Contents

1 Pin Assignments and Descriptions	4
1.1 40-Pin QFN (Top View, Through-Package)	4
1.2 QFN Pin Descriptions	4
1.3 Termination of Unused Pins	6
1.4 Electrostatic Discharge (ESD) Protection	6
2 Typical Connections Diagram	7
3 Characteristics and Specifications	8
Table 3-1. Parameter Definitions	8
Table 3-2. Recommended Operating Conditions	8
Table 3-3. Absolute Maximum Ratings	8
Table 3-4. ADC Path Characteristics	9
Table 3-5. DAC Path Characteristics	9
Table 3-6. ADC Filter Characteristics	10
Table 3-7. ADC High-Pass Filter (HPF) Characteristics	10
Table 3-8. DAC Filter Characteristics	11
Table 3-9. DAC High-Pass Filter (HPF) Characteristics	11
Table 3-10. Device Power Consumption	11
Table 3-11. Digital Interface Specifications and Characteristics	12
Table 3-12. DC Characteristics	12
Table 3-13. Switching Specifications—Reset and Clock References	13
Table 3-14. Switching Specifications—Audio Serial Port (ASP)	13
Table 3-15. Switching Specifications—I ² C Control Port	16
Table 3-16. Switching Specifications—SPI Control Port	17
4 Functional Description	18
4.1 Device Power and Reset	18
4.2 Hardware Configuration	18
4.3 Software Configuration	19
4.4 System Clocking	20
4.5 ADC and Analog Input	22
4.6 DAC and Analog Output	25
4.7 Signal-Activity Detection	27
4.8 Audio Serial Port (ASP)	28
4.9 I ² C/SPI Control Port	34
4.10 Interrupts	39
4.11 Device ID	39
5 Applications	40
5.1 Input Buffer Circuit	40
5.2 Output Buffer Circuit	41
5.3 PCB Layout Guidelines	45
5.4 Recommended Components	46
6 Register Quick Reference	49
6.1 DEVID	49
6.2 CONFIG	49
6.3 INPUT_PATH	50
6.4 OUTPUT_PATH	50
6.5 SIG_CTRL	51
6.6 PIN_CONFIG	52
6.7 IRQ_CONFIG	52
7 Register Descriptions	53
7.1 DEVID	53
7.2 CONFIG	54
7.3 INPUT_PATH	55
7.4 OUTPUT_PATH	57
7.5 SIG_CTRL	60
7.6 PIN_CONFIG	69
7.7 IRQ_CONFIG	69
8 Thermal Characteristic	72
9 Package Dimensions	72
10 Package Marking	73
11 Ordering Information	73
12 References	73
13 Revision History	74

1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top View, Through-Package)

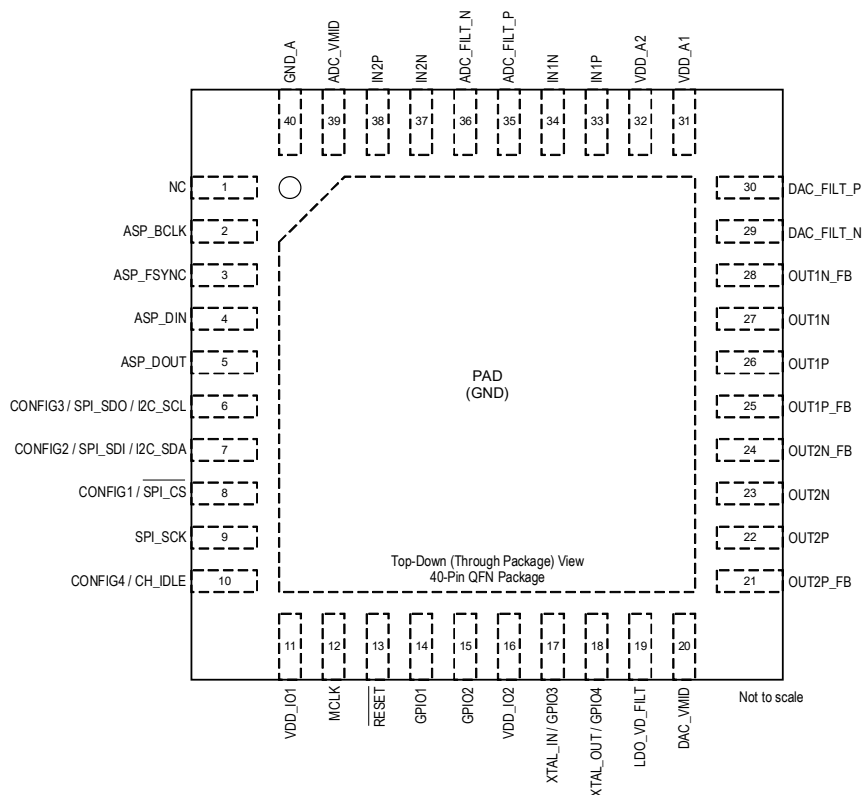


Figure 1-1. QFN 40-Pin Diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
Digital I/O				
ASP_BCLK	2	VDD_IO1	I/O	Audio serial port bit clock.
ASP_DIN	4	VDD_IO1	I	Audio serial port data input.
ASP_DOUT	5	VDD_IO1	O	Audio serial port data output.
ASP_FSYNC	3	VDD_IO1	I/O	Audio serial port frame sync.
GPIO1	14	VDD_IO2	I/O	General-purpose input/output.
GPIO2	15	VDD_IO2	I/O	General-purpose input/output.
MCLK	12	VDD_IO1	I/O	Main clock input/output.
RESET	13	VDD_IO1	I	Hardware reset control (active low).
XTAL_IN/GPIO3	17	VDD_IO2	I/O	Input for an external crystal/General-purpose input/output.
XTAL_OUT/GPIO4	18	VDD_IO2	I/O	Output for an external crystal/General-purpose input/output.
Analog I/O				
ADC_FILT_N	36	VDD_A2	O	ADC external capacitor connection.
ADC_FILT_P	35	VDD_A2	O	Connect ADC_FILT_P to VDD_A2 via a 1 Ω resistor.
ADC_VMID	39	VDD_A2	O	ADC mid-rail voltage reference output.

Table 1-1. QFN Pin Descriptions (Cont.)

Pin Name	Pin #	Power Supply	I/O	Description
CONFIG1/SPI_CS	8	VDD_IO1	I	Hardware control pins.
CONFIG2/SPI_SDI/I2C_SDA	7	VDD_IO1	I/O	In software control mode, CONFIG1 to CONFIG3 support the SPI/I2C interface.
CONFIG3/SPI_SDO/I2C_SCL	6	VDD_IO1	I/O	
CONFIG4/CH_IDLE	10	VDD_IO1	I/O	In software control mode, CONFIG1 selects the I2C target address.
SPI_SCK	9	VDD_IO1	I	In software control mode, CONFIG4 supports Signal Activity Detection. SPI clock input.
DAC_FILT_N	29	VDD_A1	O	DAC external capacitor connection.
DAC_FILT_P	30	VDD_A1	O	Connect the DAC_FILT_P capacitor to VDD_A1.
DAC_VMID	20	VDD_A1	O	DAC mid-rail voltage reference output.
IN1N	34	VDD_A2	I	Analog Input 1.
IN1P	33	VDD_A2	I	
IN2N	37	VDD_A2	I	Analog Input 2.
IN2P	38	VDD_A2	I	
LDO_VD_FILT	19	VDD_A2	O	LDO_D regulator external capacitor connection.
OUT1N	27	VDD_A1	O	Analog Output 1.
OUT1P	26	VDD_A1	O	
OUT2N	23	VDD_A1	O	Analog Output 2.
OUT2P	22	VDD_A1	O	
OUT1N_FB	28	VDD_A1	O	Analog Output 1 feedback connection.
OUT1P_FB	25	VDD_A1	O	
OUT2N_FB	24	VDD_A1	O	Analog Output 2 feedback connection.
OUT2P_FB	21	VDD_A1	O	
Power Supplies				
VDD_A1	31	—	—	Analog Supply 1.
VDD_A2	32	—	—	Analog Supply 2.
VDD_IO1	11	—	—	Digital I/O Supply 1.
VDD_IO2	16	—	—	Digital I/O Supply 2.
GND	PAD	—	—	Ground ¹ .
GND_A	40	—	—	Analog ground ¹ .
No Connect				
NC	1	—	—	No connection, it is recommended to connect to GND.

1. The GND_A pin and the ground paddle must be tied to a common ground plane directly underneath the CS4233B. It is recommended that the GND_A pin and the ground paddle are connected separately to the ground plane; the ground paddle should be connected to the ground plane using at least five vias.

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
ASP_DOUT	Float
INnX ¹	
MCLK ²	
ASP_DIN	10 kΩ pull-down to GND
ASP_FSYNC	
CONFIG3/SPI_SDO/I2C_SCL	
CONFIG4/CH_IDLE	
GPIO1	
GPIO2	
SPI_SCK	
XTAL_IN/GPIO3	
XTAL_OUT/GPIO4	
OUTnX ³	Connect to OUTnX_FB
RESET	Connect to VDD_IO1

1. See Section 5.1.1 for requirements in case of single-ended input configurations.
2. If the system clock is provided by the crystal oscillator and an MCLK output is not required, MCLK should be left floating.
3. See Section 5.2.3 for requirements in case of single-ended output configurations.

1.4 Electrostatic Discharge (ESD) Protection



ESD-sensitive device. The CS4233B is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

[illegible]

Guidance on capacitor selection is provided in [Table 2-1](#):

Connection	Capacitor	Requirements
LDO_VD_FILT	1.0 μ F ceramic	Must not derate below 0.8 μ F at 1.2 V
ADC_VMID	0.22 μ F ceramic	Must not derate below 0.1 μ F at 1.65 V
	2.2 μ F ceramic	Must not derate below 1.0 μ F at 1.65 V
ADC_FILT	0.47 μ F ceramic	Must not derate below 0.22 μ F at 3.3 V
	4.7 μ F ceramic	Must not derate below 2.2 μ F at 3.3 V
	100 μ F electrolytic	Maximum leakage current 10 μ A
DAC_FILT	22 μ F ceramic	Must not derate below 6.8 μ F at 3.3 V
DAC_VMID	0.22 μ F ceramic	Must not derate below 0.1 μ F at 1.65 V
	10 μ F ceramic	Must not derate below 5 μ F at 1.65 V
VDD_A	0.01 μ F ceramic	—
	4.7 μ F ceramic	—
VDD IO	0.1 μ F ceramic	—

3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Signal-to-noise ratio	The difference in level between the maximum full-scale output signal and the output with no input signal applied.
Dynamic range	The difference in level between the maximum full-scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied (an input signal level 60 dB below full scale is used).
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

Note: Unless specified otherwise, all performance measurements are for a 20 Hz to 20 kHz bandwidth.

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply ¹	VDD_A1, VDD_A2	3.13	3.47	V
	Digital I/O supply	VDD_IO1, VDD_IO2	1.71	3.63	V
Supply ramp up/down (all supplies)		t _{PWR-UD}	0.01	10	ms
Ambient temperature		T _A	–40	85	°C

Note: Functionality and parametric performance is not guaranteed or implied outside of the limits in this table. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise in this table): Ground = GND = GND_A = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply ¹	VDD_A1, VDD_A2	–0.3	4.32	V
	Digital core	LDO_VD_FILT	–0.3	1.52	V
	Digital I/O supply	VDD_IO1, VDD_IO2	–0.3	4.32	V
External voltage applied to digital input/output	VDD_IO1 logic pins	V _{INDI}	–0.3	VDD_IO1 + 0.3	V
	VDD_IO2 logic pins		–0.3	VDD_IO2 + 0.3	V
External voltage applied to analog inputs		V _{INAI}	–0.3	VDD_A + 0.3	V
Input current	digital input/output	I _{IN}	—	±10	mA
	analog inputs		—	±10	mA
Ambient operating temperature		T _A	–40	+115	°C
Junction operating temperature		T _J	–40	+125	°C
Storage temperature		T _{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-4. ADC Path Characteristics

Test conditions (unless specified otherwise in this table): External components as shown in Fig. 2-1 incorporating the typical input circuit illustrated in Fig. 5-1; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter		Min	Typ	Max	Units
Input impedance (INnP to INnN)	internal analog gain = 0 dB	—	12	—	kΩ
	internal analog gain = 6 dB	—	6	—	kΩ
	internal analog gain = 12 dB	—	3	—	kΩ
Full-scale differential input signal level (INnP to INnN) ¹	0 dBFS output	—	2.0	—	V _{RMS}
SNR	A-weighted	107	111	—	dB
	unweighted	104	108	—	dB
Dynamic range ²	A-weighted	—	111	—	dB
	unweighted	—	108	—	dB
THD+N ²	–1 dBFS output	—	–107	–94	dB
	–20 dBFS output	—	–87	—	dB
	–60 dBFS output	—	–47	—	dB
Input-referred noise (A-weighted)	internal analog gain = 0 dB	—	6.31	8.83	μV _{RMS}
	internal analog gain = 6 dB	—	4.47	6.25	μV _{RMS}
	internal analog gain = 12 dB	—	3.16	4.43	μV _{RMS}
CMRR	100 mV (peak-peak) 1 kHz	—	80	—	dB
Channel separation		—	110	—	dB
Interchannel phase deviation		—	0.03	—	degree
Interchannel gain deviation		—	0.1	—	dB
Gain drift		—	±100	—	ppm/°C
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	65	—	dB

1. The full-scale input signal level is also the maximum analog input level, before clipping occurs. A sinusoidal input signal is assumed.

Full-scale input signal level scales with VDD_A.

2. Performance may be affected by the input buffer, a typical input buffer circuit is illustrated in Section 5.1.

Table 3-5. DAC Path Characteristics

Test conditions (unless specified otherwise in this table): External components as shown in Fig. 2-1 incorporating the typical output circuit illustrated in Fig. 5-2; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; output load = 3 kΩ; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter		Min	Typ	Max	Units
Full scale differential output signal level (OUTnP to OUTnN)	0 dBFS input	—	2.00	—	V _{RMS}
Dynamic range	A-weighted	107	110	—	dB
	unweighted	104	107	—	dB
THD+N	0 dBFS input	—	–107	–94	dB
	–20 dBFS input	—	–87	—	dB
	–60 dBFS input	—	–47	—	dB
Idle channel noise	A-weighted	—	6.32	—	μV _{RMS}
Channel separation	1 kHz	—	110	—	dB
	20 kHz	—	100	—	dB
DC offset ¹		—	±500	—	μV
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	75	—	dB
Load resistance		3	10	—	kΩ
Load capacitance		—	—	100	pF

1. DC offset is measured between the OUTnP and OUTnN outputs.

Table 3-6. ADC Filter Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Fs = 16 kHz	Passband to –3 dB corner	—	—	0.47	Fs
	Passband ripple $f \leq 0.45 F_s$	–0.092	—	0.092	dB
	Stopband attenuation $f \geq 0.55 F_s$	98	—	—	dB
	Group delay ¹	—	20.5/Fs	—	s
Fs = 32 kHz	Passband to –3 dB corner	—	—	0.47	Fs
	Passband ripple $f \leq 0.45 F_s$	–0.092	—	0.092	dB
	Stopband attenuation $f \geq 0.55 F_s$	98	—	—	dB
	Group delay ¹	—	20.5/Fs	—	s
Fs = 44.1 kHz or 48 kHz	Passband to –3 dB corner	—	—	0.46	Fs
	Passband ripple $f \leq 0.42 F_s$	–0.099	—	0.099	dB
	Stopband attenuation $f \geq 0.58 F_s$	96	—	—	dB
	Group delay ¹	—	3.9/Fs	—	s
Fs = 88.2 kHz or 96 kHz	Passband to –3 dB corner	—	—	0.43	Fs
	Passband ripple $f \leq 0.27 F_s$	–0.011	—	0.011	dB
	Stopband attenuation $f \geq 0.77 F_s$	103	—	—	dB
	Group delay ¹	—	4.1/Fs	—	s
Fs = 176.4 kHz or 192 kHz	Passband to –3 dB corner	—	—	0.29	Fs
	Passband ripple $f \leq 0.12 F_s$	–0.010	—	0.010	dB
	Stopband attenuation $f \geq 0.67 F_s$	99	—	—	dB
	Group delay ¹	—	4.2/Fs	—	s
Fs = 352.8 kHz or 384 kHz	Passband to –3 dB corner	—	—	0.34	Fs
	Passband ripple $f \leq 0.06 F_s$	–0.010	—	0.010	dB
	Stopband attenuation $f \geq 0.94 F_s$	129	—	—	dB
	Group delay ¹	—	4.7/Fs	—	s

1. Group delay is measured from the time at which a signal is presented on the input pins (INnP/INnN) to the time of the first data bit of the corresponding FSYNC frame being output on the ASP_DOUT pin.

Table 3-7. ADC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Filter settling time		—	0.4	—	s

Table 3-8. DAC Filter Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; F_s = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
F _s = 16 kHz	Passband to –3 dB corner	—	—	0.49	Fs
	Passband ripple $f \leq 0.45 F_s$	–0.001	—	0.001	dB
	Stopband attenuation $f \geq 0.55 F_s$	100	—	—	dB
	Group delay ¹	—	33.6/Fs	—	s
F _s = 32 kHz	Passband to –3 dB corner	—	—	0.49	Fs
	Passband ripple $f \leq 0.45 F_s$	–0.001	—	0.001	dB
	Stopband attenuation $f \geq 0.55 F_s$	100	—	—	dB
	Group delay ¹	—	32.5/Fs	—	s
F _s = 44.1 kHz or 48 kHz	Passband to –3 dB corner	—	—	0.47	Fs
	Passband ripple $f \leq 0.42 F_s$	–0.004	—	0.005	dB
	Stopband attenuation $f \geq 0.59 F_s$	101	—	—	dB
	Group delay ¹	—	4.6/Fs	—	s
F _s = 88.2 kHz or 96 kHz	Passband to –3 dB corner	—	—	0.35	Fs
	Passband ripple $f \leq 0.23 F_s$	–0.001	—	0.001	dB
	Stopband attenuation $f \geq 0.55 F_s$	101	—	—	dB
	Group delay ¹	—	5.2/Fs	—	s
F _s = 176.4 kHz or 192 kHz	Passband to –3 dB corner	—	—	0.28	Fs
	Passband ripple $f \leq 0.11 F_s$	–0.001	—	0.001	dB
	Stopband attenuation $f \geq 0.55 F_s$	109	—	—	dB
	Group delay ¹	—	6.7/Fs	—	s
F _s = 352.8 kHz or 384 kHz	Passband to –3 dB corner	—	—	0.22	Fs
	Passband ripple $f \leq 0.06 F_s$	–0.001	—	0.000	dB
	Stopband attenuation $f \geq 0.55 F_s$	116	—	—	dB
	Group delay ¹	—	7.6/Fs	—	s

1. Group delay is measured from the start of the FSYNC frame containing the audio data on the ASP_DIN pin to the time at which the signal is presented on the output pins (OUTnP/OUTnN).

Table 3-9. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; F_s = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Filter settling time		—	0.4	—	s

Table 3-10. Device Power Consumption

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C; 1 kHz sine wave test signal; ASP Secondary Mode; Load capacitance (ASP_DOUT) = 20 pF; F_s = 48 kHz, 32-bit audio data.

Use Configuration	Typical Current (mA)			Total Power (mW)
	I _{VDD_A}	I _{VDD_IO1}	I _{VDD_IO2}	
Reset RESET = Logic 0	0.24	0.08	0.001	1.06
Two ADC + two DAC channels enabled	42	0.8	0.001	141.24

Table 3-11. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise in this table): Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I _{IN}	—	±10	μA
Input capacitance (per pin)		C _{IN}	—	5	pF
Digital I/O (VDD_IO1 logic pins; see Section 1)	High-level output	V _{OH}	0.9×VDD_IO1	—	V
	Low-level output	V _{OL}	—	0.1×VDD_IO1	V
	High-level input	V _{IH}	0.7×VDD_IO1	—	V
	Low-level input	V _{IL}	—	0.3×VDD_IO1	V
Digital I/O (VDD_IO2 logic pins; see Section 1)	High-level output	V _{OH}	0.9×VDD_IO2	—	V
	Low-level output	V _{OL}	—	0.1×VDD_IO2	V
	High-level input	V _{IH}	0.7×VDD_IO2	—	V
	Low-level input	V _{IL}	—	0.3×VDD_IO2	V

Table 3-12. DC Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C.

Parameter		Minimum	Typical	Maximum	Unit
LDO_VD_FILT	Nominal voltage	—	1.2	—	V
DAC_FILT	Nominal voltage	—	1.95	—	V
	VDD_A to DAC_FILT_P DAC_FILT_N to GND	—	1.9	—	V
DAC_VMID	Nominal voltage	—	1.65	—	V
	Maximum output current	—	50	—	nA
ADC_FILT	Nominal voltage	—	3.3	—	V
ADC_VMID ¹	Nominal voltage	—	1.65	—	V
	Maximum output current	—	0.01	—	mA
VDD_A power-on reset (POR) threshold (V _{POR})	VDD_A rising	2.0	—	2.8	V
	VDD_A falling	2.0	—	2.8	V
VDD_IO1 power-on reset (POR) threshold (V _{POR})	VDD_IO1 rising	1.08	—	1.58	V
	VDD_IO1 falling	0.99	—	1.43	V
VDD_IO2 power-on reset (POR) threshold (V _{POR})	VDD_IO2 rising	0.45	—	0.77	V
	VDD_IO2 falling	0.45	—	0.77	V

1. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the ADC_VMID pin. If a larger current is required, an external ADC_VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 μA), an example circuit is as follows.

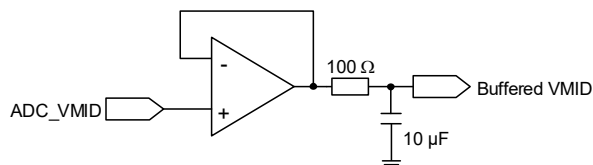


Table 3-13. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; T_A = +25 °C.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Reset	RESET low (logic 0) pulse width	t _{RLPW}	1	—	—	ms
	RESET rising edge to control port active	t _{IRS}	—	—	5	ms
MCLK input	MCLK frequency	f _{MCLK}	—	24.576	—	MHz
			—	22.5792	—	MHz
			—	49.152	—	MHz
			—	45.1584	—	MHz
	MCLK duty cycle	D _{MCLK}	45	—	55	%
	MCLK frequency tolerance	—	–1	—	1	%
MCLK output	MCLK frequency	f _{MCLK}	—	24.576	—	MHz
			—	22.5792	—	MHz
			—	49.152	—	MHz
			—	45.1584	—	MHz
	MCLK duty cycle	D _{MCLK}	45	—	55	%
	MCLK frequency accuracy	—	–1	—	1	%
Crystal	Oscillator frequency	f _{XTAL}	—	24.576	—	MHz
			—	22.5792	—	MHz
			—	49.152	—	MHz
			—	45.1584	—	MHz
	Interface transconductance	—	VDD_IO2 = 3.3 V		26	mS
			VDD_IO2 = 1.8 V		43	mS

Table 3-14. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-11); T_A = 25 °C.

Parameter 1,2,3,4,5		Symbol	Minimum	Maximum	Unit	
Secondary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC input sample/frame rate	Fs	16	384	kHz	
	ASP_FSYNC pulse width	t _{HI:FSYNC}	1/f _{ASP_BCLK}	—	ns	
	ASP_BCLK frequency	f _{BCLK}	1.024	24.576	MHz	
	ASP_BCLK high period	t _{HI:BCLK}	18	—	ns	
	ASP_BCLK low period	t _{LO:BCLK}	18	—	ns	
	ASP_FSYNC setup time before ASP_BCLK latching edge	t _{SU:FSYNC}	5	—	ns	
	ASP_FSYNC hold time after ASP_BCLK latching edge	t _{H:FSYNC}	5	—	ns	
	ASP_DIN setup time before ASP_BCLK latching edge	t _{SU:DIN}	10	—	ns	
	ASP_DIN hold time after ASP_BCLK latching	t _{H:DIN}	5	—	ns	
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	t _{D:BCLK-DOUT}	0 0	10 12	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	t _{DLY:HiZ}	0 0	9 9	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	t _{DLY:EN}	0 10	10 28	ns ns
	ASP_DOUT load capacitance	ASP_DOUT	—	0	150	pF

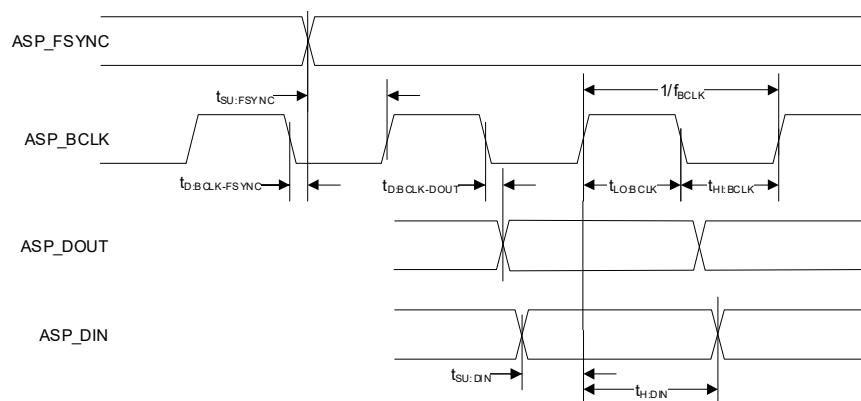
Table 3-14. Switching Specifications—Audio Serial Port (ASP) (Cont.)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-11); T_A = 25 °C.

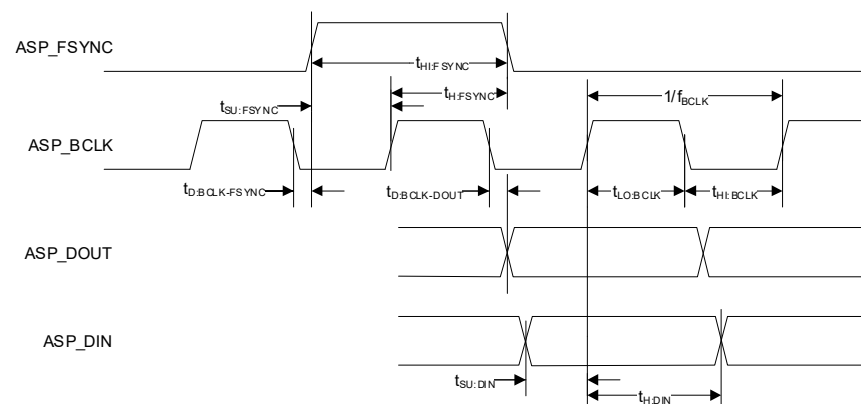
Parameter 1,2,3,4,5		Symbol	Minimum	Maximum	Unit
Primary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC output sample/frame rate	F _s	16	384	kHz
	ASP_BCLK frequency	f _{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D _{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	t _{D:BCLK-FSYNC}	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	t _{SU:DIN}	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	t _{H:DIN}	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	t _{D:BCLK-DOUT}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 11	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge		half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 10	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	t _{DLY:EN}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 15	ns ns
	ASP_x load capacitance		ASP_BCLK ASP_FSYNC ASP_DOUT	0 0 0	pF pF pF
		—	0	50	pF
Secondary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC input sample/frame rate	F _s	16	384	kHz
	ASP_FSYNC pulse width	t _{HI:FSYNC}	1/f _{ASP_BCLK}	—	ns
	ASP_BCLK frequency	f _{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period	t _{HI:BCLK}	18	—	ns
	ASP_BCLK low period	t _{LO:BCLK}	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	t _{SU:FSYNC}	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	t _{H:FSYNC}	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	t _{SU:DIN}	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	t _{H:DIN}	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	t _{D:BCLK-DOUT}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 15	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge		half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 12	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	t _{DLY:EN}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 11	ns ns
	ASP_DOUT load capacitance		ASP_DOUT	0	pF
		—	0	150	pF
Primary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC output sample/frame rate	F _s	16	384	kHz
	ASP_BCLK frequency	f _{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D _{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	t _{D:BCLK-FSYNC}	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	t _{SU:DIN}	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	t _{H:DIN}	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	t _{D:BCLK-DOUT}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 16	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge		half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 13	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	t _{DLY:EN}	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	0 7	ns ns
	ASP_x load capacitance		ASP_BCLK ASP_FSYNC ASP_DOUT	0 0 0	pF pF pF
		—	0	50	pF

1. The ASP_BCLK launching edge is selectable. Half-cycle mode = ASP_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP_BCLK launching edge is same as latching edge.

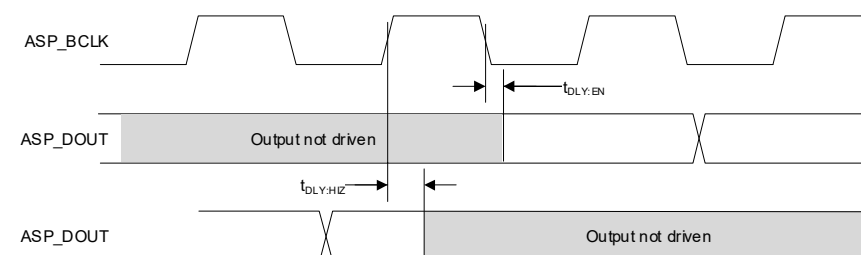
2. ASP timing in I²S and Left-Justified Modes.
 ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



3. ASP timing in TDM Mode.
 ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



4. ASP_DOUT timing for multiple devices sharing the audio serial port bus—half-cycle mode.



5. ASP_DOUT timing for multiple devices sharing the audio serial port bus—full-cycle mode.

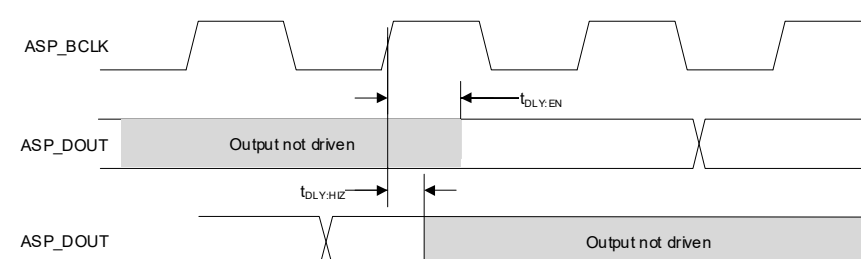


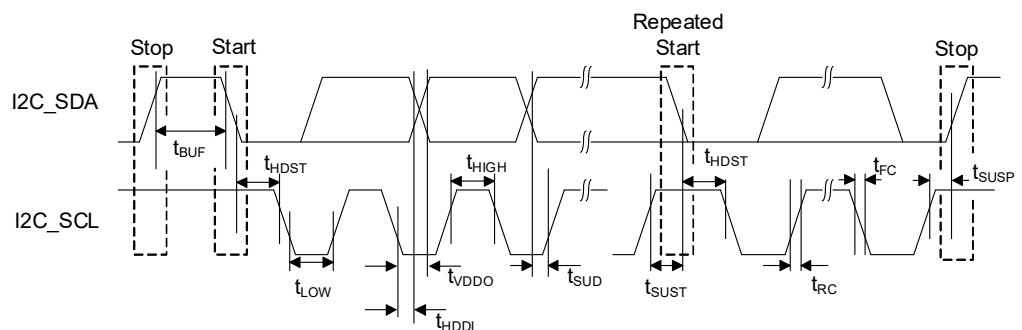
Table 3-15. Switching Specifications—I2C Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-11); T_A = 25 °C.

Parameter 1,2	Symbol	Minimum	Maximum	Unit	
SCL clock frequency	f _{SCL}	—	1000	kHz	
Clock low time	t _{LOW}	500	—	ns	
Clock high time	t _{HIGH}	260	—	ns	
Start condition hold time (before first clock pulse)	t _{HDST}	260	—	ns	
Setup time for repeated start	t _{SUST}	260	—	ns	
Rise time of SCL and SDA	t _{RC}	f _{SCL} ≤ 100 kHz	600	1000	ns
		100 kHz < f _{SCL} ≤ 400 kHz	180	300	ns
		400 kHz < f _{SCL} ≤ 1000 kHz	72	120	ns
Fall time of SCL and SDA	t _{FC}	f _{SCL} ≤ 100 kHz	6.5	300	ns
		100 kHz < f _{SCL} ≤ 400 kHz	6.5	300	ns
		400 kHz < f _{SCL} ≤ 1000 kHz	6.5	120	ns
Rise time variation between SDA and SCL	—	—	1.67	ns	
Fall time variation between SDA and SCL	—	f _{SCL} ≤ 100 kHz	—	100	ns
		100 kHz < f _{SCL} ≤ 400 kHz	—	100	ns
		400 kHz < f _{SCL} ≤ 1000 kHz	—	75	ns
Setup time for stop condition	t _{SUSP}	260	—	ns	
SDA setup time to SCL rising	t _{SUD}	50	—	ns	
SDA input hold time from SCL falling ³	t _{HDDI}	0	—	ns	
Output data valid (Data/ACK) ⁴	t _{VDDO}	f _{SCL} ≤ 100 kHz	—	3450	ns
		100 kHz < f _{SCL} ≤ 400 kHz	—	900	ns
		400 kHz < f _{SCL} ≤ 1000 kHz	—	450	ns
Bus free time between transmissions	t _{BUF}	500	—	ns	
SDA bus capacitance	C _B	—	550	pF	
SCL/SDA pull-up resistance	R _P	500	—	Ω	
Pulse width of spikes to be suppressed	t _{ps}	0	50	ns	

1. All timing is relative to thresholds specified in Table 3-11, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.

2. I2C control-port timing.



3. Data must be held long enough to bridge the transition time, t_{FC}, of SCL.

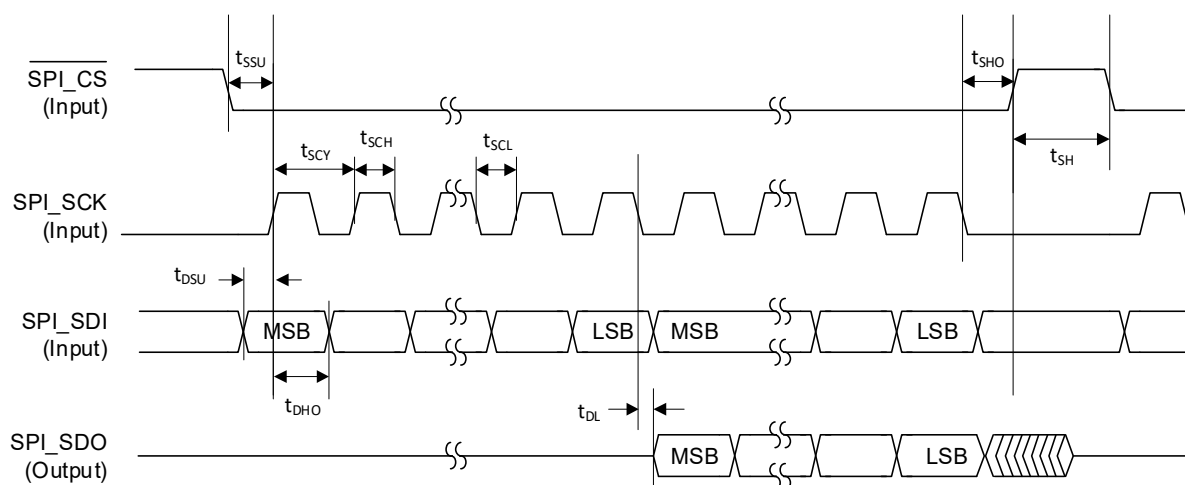
4. Time from falling edge of SCL until data output is valid.

Table 3-16. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-11); T_A = 25 °C.

Parameter ¹	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f _{SCY}	—	24	MHz
SPI_CS falling edge to SPI_SCK rising edge	t _{SSU}	5	—	ns
SPI_SCK falling edge to SPI_CS rising edge	t _{SHO}	0.5	—	ns
SPI_SCK pulse width low	t _{SCL}	18.5	—	ns
SPI_SCK pulse width high	t _{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t _{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t _{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t _{DL}	0	15	ns
SPI_CS rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active SPI_CS	t _{SH}	20	—	ns

1. SPI control-port timing.



4 Functional Description

4.1 Device Power and Reset

The CS4233B is powered using VDD_A1, VDD_A2, VDD_IO1, and VDD_IO2 external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be star-connected and powered from a single supply. The associated power domain is referred to as VDD_A.

VDD_IO1 and VDD_IO2 are independent power domains. VDD_IO1 supplies host-related interfaces (e.g., SPI control interface); VDD_IO2 supplies external interfaces (e.g., crystal oscillator connections). Integrated level shifters are included for direct interface to logic levels from 1.8 V to 3.3 V.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS4233B is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A supply is below the respective reset threshold defined in [Table 3-12](#).

The GND_A pin and the ground paddle, must be tied to a common ground (GND) plane directly underneath the CS4233B.

4.2 Hardware Configuration

The CS4233B supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in [Table 4-1](#). See [Section 4.4](#) for more details of the sample-rate selection and [Section 4.8](#) for more details of the ASP operation.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration	Description
CONFIG1	Pull-up to VDD_IO1	0 Ω Software control mode (I ² C/SPI)
		4.7 k Ω In I ² C Mode, the pull-up resistor is used to select the device address—see Section 4.9 .
		22 k Ω In SPI Mode, it is recommended to use a 100 k Ω pull-up resistor.
		100 k Ω
	Pull-down to GND	100 k Ω ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
		22 k Ω ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 k Ω ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω ASP Secondary Mode, autodetect sample rate
CONFIG2	Pull-up to VDD_IO1	0 Ω ASP TDM Mode—minimum time slots ¹ , ASP_FSYNC_TYPE = pulse
		4.7 k Ω ASP TDM Mode—maximum time slots ² , data output on BCLK falling edge (half-cycle mode) ³ , ASP_FSYNC_TYPE = pulse
		22 k Ω ASP TDM Mode—maximum time slots ² , data output on BCLK rising edge (full-cycle mode) ⁴ , ASP_FSYNC_TYPE = pulse
		100 k Ω ASP TDM Mode—minimum time slots ¹ , ASP_FSYNC_TYPE = square wave (50% duty cycle) ⁵
	Pull-down to GND	100 k Ω ASP TDM Mode—maximum time slots ² , data output on BCLK falling edge (half-cycle mode) ³ , ASP_FSYNC_TYPE = square wave (50% duty cycle) ⁵
		22 k Ω ASP TDM Mode—maximum time slots ² , data output on BCLK rising edge (full-cycle mode) ⁴ , ASP_FSYNC_TYPE = square wave (50% duty cycle) ⁵
		4.7 k Ω ASP Left-Justified Mode
		0 Ω ASP I ² S Mode

1. The ASP data format is configured to support two time slots; this is the minimum necessary for the CS4233B input/output.

2. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate, refer to [Table 4-13](#).

3. Half-cycle mode = ASP_DOUT launching edge (BCLK falling) is opposite to the receiving-device latching edge (BCLK rising), refer to [Table 3-14](#).

4. Full-cycle mode = ASP_DOUT launching edge (BCLK rising) is same as the receiving-device latching edge, refer to [Table 3-14](#).

5. [ASP_FSYNC_TYPE](#) = square wave (50% duty cycle) is available in ASP Primary Mode only, as described in [Section 4.8](#).

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in [Table 4-2](#). See [Section 4.8](#) for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO1	0 Ω	Slots 14–15 [1]
		4.7 k Ω	Slots 12–13 [1]
		22 k Ω	Slots 10–11 [1]
		100 k Ω	Slots 8–9 [1]
	Pull-down to GND	100 k Ω	Slots 6–7 [2]
		22 k Ω	Slots 4–5 [2]
		4.7 k Ω	Slots 2–3
		0 Ω	Slots 0–1

1. Slots 8–15 are only valid in 16-slot TDM Mode.

2. Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference and virtual PAD configurations are determined using the CONFIG4 pin as described in [Table 4-3](#). See [Section 4.4](#) for more details of the CS4233B clocking architecture, and [Section 4.5.5](#) for more details of virtual PAD function.

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz) ¹	Virtual PAD
CONFIG4	Pull-up to VDD_IO1	0 Ω	XTAL	49.152 or 45.1584	Bypassed
		4.7 k Ω	XTAL	24.576 or 22.5792	
		22 k Ω	MCLK	49.152 or 45.1584	
		100 k Ω	MCLK	24.576 or 22.5792	
	Pull-down to GND	100 k Ω	MCLK	49.152 or 45.1584	Enabled - Level Detection
		22 k Ω	MCLK	24.576 or 22.5792	
		4.7 k Ω	MCLK	49.152 or 45.1584	Enabled - Edge Detection ²
		0 Ω	MCLK	24.576 or 22.5792	

1. The reference clock frequency is related to sample rate options (for supported configurations, see [Section 4.4](#)).

2. If CONFIG4 is configured for virtual PAD edge-detection switching, the GPIO1 pin is configured as a logic output; in this case, the DAC shutdown function is not supported (for details of DAC shutdown, see [Section 4.6.4](#))

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 is pulled-up to VDD_IO1), the device configuration is controlled by register writes via the applicable control interface, as described in [Section 4.9](#). Unused CONFIGx pins should be terminated as described in [Section 1.3](#).

Note: In software mode, the CONFIG1 pin is used to select the I²C target address (see [Section 4.9](#)). If the SPI control interface is used, it is recommended to connect the CONFIG1 pin to VDD_IO1 via a 100 k Ω resistor.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is pulled-up to VDD_IO1; note that $\overline{\text{RESET}}$ must remain asserted (i.e., Logic 0) until CONFIG_1/SPI_CS is deasserted (i.e., Logic 1). In software control mode, the CS4233B is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG1 pin. See [Section 4.9](#) for further details of the I²C/SPI control port.

In software control mode, **GLOBAL_EN** is used as the global control field for enabling/disabling the CS4233B functions. The device should be configured using the applicable control registers before setting **GLOBAL_EN**.

Notes: The clocking (Section 4.4) and ASP (Section 4.8) control registers are only valid on the rising edge of **GLOBAL_EN**. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (**GLOBAL_EN** = 0) before writing to these registers.

To minimize the CS4233B power consumption when all output paths are disabled, see Section 4.6.4.

A reset of the CS4233B can be triggered by writing 0x5A to the **SW_RESET** field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS4233B is provided using either the MCLK input or the crystal (XTAL) oscillator. In each case, the frequency is related to sample rate options, as described in Table 4-4:

Table 4-4. Reference Frequency and Sample Rate Options

Reference Source	Reference Frequency (MHz)	Sample Rate (kHz) ¹
MCLK or XTAL	22.5792 or 45.1584	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152	16, 32, 48, 96, 192, 384

1. Sample rates 352.8 kHz and 384 kHz are supported in software control mode only (for details of software control mode, see Section 4.4.2).

The specifications for the clocking sources are described in Table 3-13; for optimal out-of-band noise performance a reference frequency of 49.152 MHz or 45.1584 MHz is recommended.

In hardware mode, the clock source is configured using the CONFIG4 pin, as detailed in Table 4-3. In software mode, the clocking source is selected using **SYSCLK_SRC**.

The crystal oscillator uses an external crystal to generate the system clock. Load capacitors are connected to the crystal as shown in Fig. 4-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

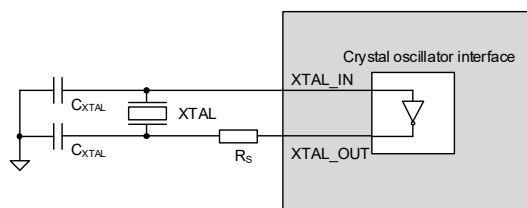


Figure 4-1. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.4.1. The suitability of the external crystal is calculated as a function of the operating voltage (V_{DD_IO2}) and the transconductance of the crystal interface, as defined in Table 3-13.

If clocking is provided using the crystal oscillator, the CS4233B outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

In ASP Secondary Mode, the ASP_FSYNC input is used to control the ADC-sample and DAC-conversion timing, enabling multiple CS4233B devices to operate synchronously (sample timing is phase aligned) in a system. The external clocks ASP_FSYNC and ASP_BCLK must be derived from a common clock source (i.e., the MCLK input, or the MCLK output when clocking is provided using the crystal oscillator). See Section 4.8 for more details of the ASP.

The clocking architecture is illustrated in [Fig. 4-2](#).

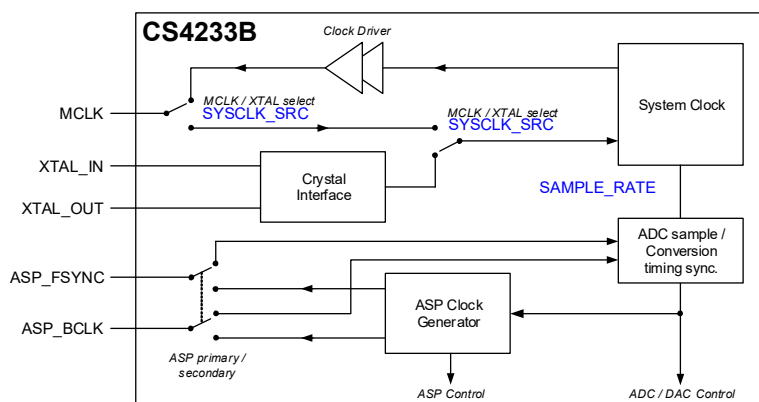


Figure 4-2. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the system clock can be sourced from the MCLK pin or from the crystal oscillator. In each case, the frequency must be:

- 49.152 MHz or 24.576 MHz for sample rates of 16, 32, 48, 96, or 192 kHz
- 45.1584 MHz or 22.5792 MHz for sample rates of 44.1, 88.2, or 176.4 kHz

The clock source is configured using the CONFIG4 pin as described in [Section 4.2](#).

The sample rate is selected using the CONFIG1 pin as described in [Section 4.2](#). Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (sample rates 16 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. The autodetect sample-rate option is only valid if the ASP is operating in Secondary Mode (see [Section 4.8](#)).

The supported clocking configurations are summarized in [Table 4-5](#).

Table 4-5. System Clock Configuration

Reference Source	Reference Frequency (MHz)	ASP Operating Conditions ¹
MCLK or XTAL	24.576 or 49.152	Primary or Secondary Mode, I ² S, left-justified, or TDM data formats, sample rates 48, 96, and 192 kHz Primary Mode, or sample rates 16, 32, 48, 96, and 192 kHz in Secondary Mode (autodetect only).
MCLK or XTAL	22.5792 or 45.1584	Primary or Secondary Mode, I ² S, left-justified, or TDM data formats, sample rates 44.1, 88.2, and 176.4 kHz in Primary Mode, or sample rates 44.1, 88.2, 176.4 kHz in Secondary Mode (autodetect only).

¹. See [Section 4.8](#) for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in [Table 4-6](#).

Table 4-6. Hardware Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4
	24.576 or 49.152		16, 32, 48, 96, 192
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS4233B is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4233B MCLK output, see [Section 4.8](#).

4.4.2 Software Control Mode

In software (I²C/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using [SAMPLE_RATE](#). Sample rates 16 kHz–384 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample-rate autodetect option is only valid for sample rates 16 kHz–192 kHz.
- The system clock source is selected using [SYSCLK_SRC](#). The clock source can be either the crystal oscillator or MCLK.
- The system clock frequency is configured using [SYSCLK_FREQ](#). The system clock frequency must be
 - 49.152 MHz or 24.576 MHz for sample rates of 16, 32, 48, 96, 192, or 384 kHz
 - 45.1584 MHz or 22.5792 MHz for sample rates of 44.1, 88.2, 176.4, or 352.8 kHz.

The sample rate must be related to the system clock reference as described in [Table 4-7](#).

Table 4-7. Software Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152		16, 32, 48, 96, 192, 384
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192, 384

The sample-rate autodetect option (16 kHz–192 kHz) is only valid if the ASP is operating in Secondary Mode (see [Section 4.8](#)).

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS4233B is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4233B MCLK output, see [Section 4.8](#).

4.5 ADC and Analog Input

The CS4233B supports two analog input channels, each incorporating a high-performance sigma-delta analog-to-digital converter (ADC) with integrated programmable analog gain. Digital volume and mute control is also provided on each input channel.

The analog gain, digital volume, and mute controls are supported in software (I²C/SPI) control mode only.

4.5.1 ADC Path Enable

The analog input and ADC paths are enabled using [INx_ADC_EN](#) (where x indicates the channel number 1–2).

Note: Both input paths (1–2) must always be configured in the same state (enabled or disabled). For example, input path 1 should not be enabled without also enabling input path 2.

The polarity of the ADC output can be inverted using [INx_INV](#) for the respective channel.

4.5.2 ADC Digital Volume and Mute

The ADC signal path incorporates a digital volume control, supporting a range of –127.5 dB to +30 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using [INx_VOL](#) for the respective input channel. The digital mute is enabled by setting [INx_MUTE](#).

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to [IN_VU](#). Writing 1 to [IN_VU](#) causes the volume and mute settings to be updated on all input paths simultaneously.

When the volume or mute is changed, the digital gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by [IN_RAMP_RATE_INC](#); for decreasing gain, the rate is controlled by [IN_RAMP_RATE_DEC](#).

Note: The [IN_RAMP_RATE_INC](#) and [IN_RAMP_RATE_DEC](#) fields should not be changed while a volume ramp is in progress.

4.5.3 Input Path Analog and Digital Gain

The ADC signal path incorporates analog gain, minimizing external component requirements. The analog gain enhances overall system efficiency and performance by delivering superior input-referred noise and maintaining signal integrity between different applications.

The analog gain is configurable to 0 dB, 6 dB, or 12 dB. The maximum differential input signal level at each gain setting is shown in [Table 4-8](#).

Table 4-8. Maximum Input Signal Level per Internal Analog Gain Setting

Internal Analog Gain (dB)	Maximum Input Signal Level (V_{RMS})
0	2
6	1
12	0.5

The ADC path incorporates digital gain, supporting a range of –32 dB to +31.875 dB in 0.125 dB steps. The digital gain provides fine adjustment of the overall input path gain, optimizing the dynamic range of the signal path across a wide range of signal levels.

4.5.3.1 Gain Control

Zero-cross detection is used to synchronize the analog and digital gain changes, avoiding audible gain-change transients.

The analog gain is configured for each channel using the respective [IN_x_INT_ANA_GAIN](#) bit (where x indicates the channel number 1–2). If enabled, both channels are configured with 0 dB gain by default.

The digital gain is configured for each channel using [IN_x_INT_DIG_GAIN](#).

The gain changes are applied upon register write using [IN_x_UPDATE](#).

Note: The digital volume and digital gain are configured separately. The total digital gain of the input path is the sum of the digital volume and digital gain. Digital volume is described in [Section 4.5.2](#).

4.5.4 Input Clip Warning

The CS4233B provides a clip-warning function on the ADC input paths; this can be used to provide a warning of large or clipped signal levels.

The clip-warning threshold level is configured using [IN_CLIP_THRESH](#). The selected level applies to both input channels.

Clip warning provides input to the interrupt controller (see [Section 4.10](#)). If an input signal exceeds the clip-warning threshold, the [IN_x_CLIP_WARN_INT](#) bit is set (where x indicates the channel number 1–2). These bits are latching fields which, once set, remain set until a 1 is written to the respective bits; these bits can be polled at any time or in response to the IRQ output signal being asserted.

4.5.5 Virtual PAD

The CS4233B includes a virtual PAD function that emulates a conventional PAD with minimal impact on the noise floor; this reduces external component requirements, leading to a more compact and efficient design.

If virtual PAD is used, an external preamplifier attenuates the input signal, emulating a PAD-on status. To emulate a PAD-off status, corresponding gain is applied to compensate for the external attenuation. This architecture ensures a consistent anti-aliasing filter response in either state.

A logic input to a GPIO pin can be used to select PAD-on/off status. In software mode, the PAD-on/off status can also be selected by writing to control registers via the applicable control interface.

If a logic input to a GPIO pin is used to select PAD-on/off status, edge or level detection is supported.

- If edge detection is selected, a rising-edge input on a GPIO pin toggles the PAD-on/off status for each channel. The PAD-on/off status for each channel is provided as a logic output on a GPIO pin; this can be used, for example, to control LEDs for visual indication. The Logic 1 output indicates the PAD-off status; the Logic 0 output indicates the PAD_on status.
- If level detection is selected, a Logic 1 input on a GPIO pin selects PAD-off status and a Logic 0 input selects PAD-on status; a logic output is not provided. The logic levels are described in [Table 3-11](#).

Note: The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see [Table 3-11](#) for details).

Virtual PAD is supported in hardware and software modes.

4.5.5.1 Hardware Mode

In hardware mode, the virtual PAD function supports a fixed external attenuation of 20 dB. The CS4233B analog and digital gains are configured to provide +20 dB gain if PAD-off status is selected and 0 dB gain if PAD-on status is selected.

Note: Virtual PAD is only supported in hardware mode if the system clock is sourced from MCLK.

Edge or level detection is configured using the CONFIG 4 pin, as shown in [Table 4-3](#).

If edge detection is selected, the GPIO pins as assigned as described in [Table 4-9](#).

Table 4-9. Virtual PAD Edge Detection GPIO Configuration

Pin Number	Pin Name	Function
14	GPIO1	Channel 1 output
15	GPIO2	Channel 2 output
17	GPIO3	Channel 1 input
18	GPIO4	Channel 2 input

If level detection is selected, the GPIO pins are assigned as described in [Table 4-10](#).

Table 4-10. Virtual PAD Level Detection GPIO Configuration

Pin Number	Pin Name	Function
14	GPIO1	DAC shutdown input
15	GPIO2	—
17	GPIO3	Channel 1 input
18	GPIO4	Channel 2 input

Note: If edge detection is selected, the DAC shutdown function is not available. For further details on DAC shutdown refer to [Section 4.6.4](#).

4.5.5.2 Software Mode

In software mode, the virtual PAD function supports a range of fixed external preamplifier gains; for PAD-on, a maximum attenuation of 20 dB is supported.

- To emulate PAD-off status, the internal analog and digital gains are configured for each channel using [INx_HIGH_INT_ANA_GAIN](#) and [INx_HIGH_INT_DIG_GAIN](#) respectively (where x indicates the channel number 1–2).
- To emulate PAD-on status, the internal analog and digital gains are configured using [INx_LOW_INT_ANA_GAIN](#) and [INx_LOW_INT_DIG_GAIN](#) respectively.

The gain configuration settings do not take effect until the PAD-on/off status is selected. PAD-off status can be selected by writing 1 to [INx_HIGH_UPDATE](#); PAD-on status can be selected by writing 1 to [INx_LOW_UPDATE](#).

PAD-on/off selection provides input to the interrupt controller, described in [Section 4.10](#). If [INx_HIGH_UPDATE](#) and [INx_LOW_UPDATE](#) are set concurrently (i.e., PAD-on status and PAD-off status are both selected simultaneously), an interrupt event is indicated using [GAIN_CONFLICT_INT](#). This is a latching bit which, once set, remains set until a 1 is written. This bit can be polled at any time or in response to the IRQ output signal being asserted.

The PAD-on/off status can be selected by a logic input to a GPIO pin; the pin is selected using the respective [INx_GPI_SEL](#) bits. Edge or level detection (described in [Section 4.5.5](#)) is configured using [SW_TYPE](#); the debounce time is configurable using [DB_TIME](#).

- If edge detection is selected, the input polarity can be inverted for each channel using the respective [INx_GPI_POL](#) bits.
- If level detection is selected, a Logic 1 input selects PAD-off status and a Logic 0 input selects PAD-on status.

The PAD-on/off status for each channel can be configured as a logic output on a GPIO pin; the pin is selected using the respective [INx_GPO1_SEL](#) to [INx_GPO4_SEL](#) bits. For PAD-on status, the GPIO output level (i.e. Logic 0 or Logic 1) status is configured using [INx_LOW_GPO1](#) to [INx_LOW_GPO4](#); for PAD-off status, the GPIO output level is configured using [INx_HIGH_GPO1](#) to [INx_HIGH_GPO4](#).

Notes: Pins GPIO3 and GPIO4 are not available if the system clock is sourced from the crystal oscillator.

The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see [Table 3-11](#) for details).

The current status for each GPIO pin is indicated using [GPI_STS](#) and [GPO_STS](#). If the input polarity is inverted (i.e., the [INx_GPI_POL](#) bits are set), the [GPI_STS](#) bits indicate the opposite logic level to the GPIO pin status.

4.5.5.3 Automatic PAD Response

In software mode, the virtual PAD function incorporates a level detector on the ADC input channels to selectively determine whether the PAD should be turned on. This can be used to prevent clipping of large signals at the ASP output without requiring host intervention. The level detector is enabled on each audio channel using the respective [INx_PAD_LD_EN](#) bit (where x indicates the channel number 1–2).

Signal detection for the high-level threshold uses either the instantaneous or averaged signal level; this is selected using [IN_PAD_LD_AVG](#). Signal detection for the low-level threshold uses the averaged signal level. The averaged signal level is calculated using an exponential moving average (EMA) function; the time constant is configurable using [IN_PAD_LD_TIME](#).

The high and low thresholds associated with the virtual PAD level detector are configured using [INx_PAD_HIGH_THR](#) and [INx_PAD_LOW_THR](#) respectively.

Note: Thresholds described in [INx_PAD_HIGH_THR](#) are for signal detection using the averaged signal level; if the instantaneous signal level is selected, the thresholds are approximately 4 dB lower than stated.

If the input signal exceeds the high-level threshold, the CS4233B can automatically select PAD-on status. Automatic PAD response is enabled using [INx_PAD_AUTO_EN](#). Note that PAD-on status remains selected until PAD-off is selected by a Logic 1 input to a GPIO pin or by writing 1 to [INx_HIGH_UPDATE](#).

Automatic PAD response provides input to the interrupt controller, described in [Section 4.10](#). If the input signal exceeds the low-level threshold, the [INx_PAD_LOW_INT](#) bit is set. If the input signal exceeds the high-level threshold, the [INx_PAD_HIGH_INT](#) bit is set. These bits are latching fields which, once set, remains set until a 1 is written. These bits can be polled at any time or in response to the IRQ output signal being asserted; the host can use these bits to determine whether to turn the PAD-on, or to turn the PAD-off (including after an automatic response).

4.6 DAC and Analog Output

The CS4233B supports up to two analog output channels, each incorporating a high-performance sigma-delta digital-to-analog converter (DAC). Digital volume and mute control is provided on each output channel.

The digital volume and mute controls are supported in software (I²C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB volume.

4.6.1 DAC Path Enable

The analog outputs and DAC paths are enabled using `OUTx_DAC_EN` (where x indicates the channel number 1–2).

When the output paths are enabled for the first time after power-up or after the DAC reference has been disabled (described in [Section 4.6.4](#)), the paths do not become active until a startup delay has elapsed; the delay ensures the noise floor of the output path has settled before it becomes active and mitigates any audible artifacts. The time delay (1 s) is applied when the output paths are enabled using `OUTx_DAC_EN`.

The polarity of the DAC output can be inverted using `OUTx_INV` for the respective channel.

The CS4233B supports a mono output configuration; this can be used in applications where stereo sound is unnecessary, such as voice playback, alarms, or devices with a single speaker. If mono operation is required, it is recommended to configure the CS4233B with a single output path enabled prior to initial startup to minimize any audible artifacts.

4.6.2 DAC Digital Volume and Mute

The DAC signal path incorporates a digital volume control, supporting a range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using `OUTx_VOL` for the respective output channel. The digital mute is enabled by setting `OUTx_MUTE`.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to `OUT_VU`. Writing 1 to `OUT_VU` causes the volume and mute settings to be updated on all output paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by `OUT_RAMP_RATE_INC`; for decreasing gain, the rate is controlled by `OUT_RAMP_RATE_DEC`.

Note: The `OUT_RAMP_RATE_INC` and `OUT_RAMP_RATE_DEC` fields should not be changed while a volume ramp is in progress.

4.6.3 DAC Power Optimization

A Class A amplifier is provided in the DAC output path to convert the current output to a voltage output. An external feedback circuit is required, as described in [Section 5.2](#).

A voltage output of 2 V_{RMS} is provided; this supports a minimum resistive load of 3 kΩ in parallel with a maximum capacitive load of 100 pF. If the load has a higher impedance, the CS4233B can optimize power consumption by adjusting the drive current while maintaining an output of 2 V_{RMS}. In this case, a minimum resistive load of 10 kΩ in parallel with a maximum capacitive load of 100 pF is supported.

The maximum load impedance is selected using `OUT_LOAD_CFG`.

4.6.4 DAC Shutdown

To minimize power consumption when all output paths are disabled, the DAC reference circuit can be disabled. Note that power consumption is only reduced if the output paths have previously been enabled. Until they are enabled for the first time, the power consumption is already minimized.

In software mode, the DAC reference circuit is disabled using `DAC_SHUTDOWN`. If this bit is set, all paths are disabled regardless of the status of the `OUTx_DAC_EN` bits. Prior to disabling the DAC reference circuit, it is recommended to mute the output paths, as described in [Section 4.6.2](#).

Note: If the `DAC_SHUTDOWN` bit is cleared, any output paths where `OUTx_DAC_EN` is set are enabled.

In hardware mode, the DAC shutdown function incorporates a controlled shutdown sequence to mitigate any audible artifacts. The shutdown sequence slowly ramps down the digital volume and then ramps down the DAC output voltage prior to disabling the DAC reference circuit.

The shutdown sequence is selected using a rising-edge logic input on the GPIO1 pin. GPIO1 must be held low (i.e., Logic 0) during device startup.

Note: If CONFIG4 is configured to enable virtual PAD edge detection (refer to [Table 4-3](#)), GPIO1 functions as a GPIO output. In this case, the DAC shutdown function is not available in hardware mode. For further details on virtual PAD see [Section 4.5.5](#).

To enable the DAC reference circuit after a hardware shutdown the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled.

4.7 Signal-Activity Detection

The CS4233B incorporates a signal-activity detection function on the ADC input paths and DAC output paths. Signal-activity detection controls the logic level condition of the CH_IDLE output pin—the Logic 0 condition indicates signal activity on one or more input; the Logic 1 condition indicates no signal activity on all inputs.

The CH_IDLE pin is an open-drain output, allowing multiple devices to drive the Logic 0 condition in a wired-OR configuration. In a typical application, the host monitors the CH_IDLE logic level condition to determine the input signal-activity status. An external pull-up resistor, typically 10 k Ω , is required on the CH_IDLE pin.

Signal activity is detected on enabled ADC input channels and on the ASP input data stream of enabled DAC output paths; controls such as volume and mute have no effect on signal-activity detection. If any input channels are disabled using [INx_ADC_EN](#) or if any output paths are disabled using [OUTx_DAC_EN](#) or [DAC_SHUTDOWN](#), signal activity on the disabled path(s) does not contribute to the logic-level condition of the CH_IDLE output pin.

Signal-activity detection is enabled independently on the ADC input paths and the DAC output paths by writing 0x3 to [IN_SIG_ACT_EN](#) and [OUT_SIG_ACT_EN](#) respectively.

If signal-activity detection is enabled on the ADC input paths, the signal level on each channel is monitored against configurable high- and low-level thresholds. The high-level threshold for each channel is configured using the respective [INx_SIG_ACT_HIGH_THR](#) bits (where x indicates the channel number 1–2); the low-level threshold for each channel is configured using [INx_SIG_ACT_LOW_THR](#). If signal-activity detection is enabled only on the ADC paths, the CH_IDLE behavior is:

- If the signal level on any input channel exceeds the high-level threshold, CH_IDLE is driven low (Logic 0).
- If the signal level on all input channels falls below the low-level threshold, CH_IDLE is pulled high (Logic 1).

If signal-activity detection is enabled on the DAC output paths, the input signal level for each DAC output channel is monitored against a configurable signal-activity threshold. The threshold is configured for each channel using the respective [OUTx_SIG_ACT_THR](#) bits. If signal-activity detection is enabled only on the DAC output paths, the CH_IDLE behavior is:

- If the input signal level for any output path exceeds the signal-activity threshold, CH_IDLE is driven low (Logic 0).
- If the input signal level for all output paths falls below the signal-activity threshold, CH_IDLE is pulled high (Logic 1).

If signal-activity detection is enabled on both the ADC input paths and the DAC output paths, the CH_IDLE behavior is:

- If the signal level on any ADC input channel exceeds the high-level threshold or if the input signal level for any DAC output channel exceeds the signal-activity threshold, CH_IDLE is driven low (Logic 0).
- If the signal level on all ADC input channels falls below the low-level threshold and if the input signal level for all DAC output channels falls below the signal-activity threshold, CH_IDLE is pulled high (Logic 1).

Signal-activity detection uses an averaged signal level that is calculated using an exponential moving average (EMA) function. The EMA function for each ADC input channel is enabled using [INx_EMA_EN](#) respectively; the EMA function for each DAC output channel is enabled automatically when signal-activity detection is enabled on the DAC paths.

The EMA time constant is configured independently for the ADC input paths and DAC output paths. The time constant for the ADC input paths is selected using [IN_EMA_TIME](#); the time constant for the DAC output paths is selected using [OUT_EMA_TIME](#).

If signal-activity detection is enabled on the ADC input paths and the EMA function for any input channel is disabled, signal activity on that channel will not be detected—CH_IDLE will not be driven low (Logic 0) by signal activity on that channel. It is recommended to enable the EMA function for all input channels.

4.8 Audio Serial Port (ASP)

The multichannel ASP supports the input/output of digital audio samples to/from the CS4233B. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats.

Timing specifications for the ASP are described in [Table 3-14](#). An option is supported to drive the output data (DOUT) on the rising or falling BCLK edge; driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS4233B and the sampling edge at the receiving device.

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see [Section 4.2](#)). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 16 kHz–192 kHz are supported (sample rates 16 kHz and 32 kHz are supported using autodetect in ASP Secondary Mode only). In software mode, sample rates 16 kHz–384 kHz are supported; sample rate 384 kHz is not supported by autodetect. The supported sample rates in ASP Primary Mode and ASP Secondary Mode are summarized in [Table 4-11](#).

Table 4-11. Supported Sample Rates in ASP Primary Mode and ASP Secondary Mode

Sample Rate (kHz)	ASP Primary Mode		ASP Secondary Mode	
	Hardware Control Mode	Software Control Mode	Hardware Control Mode	Software Control Mode
16–32	—	Configurable using SAMPLE_RATE	Determined using autodetect only	Configurable using SAMPLE_RATE (autodetect available)
44.1–192	Determined by CONFIG1 pin			
352.8, 384	—		—	Configurable using SAMPLE_RATE (autodetect not available)

4.8.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS4233B. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge.

If clocking is provided by the crystal oscillator and the CS4233B is operating in ASP Secondary Mode, then the FSYNC and the BCLK signals should be derived from the common clock source provided by the CS4233B MCLK output.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see [Section 4.2](#)). In software control mode, the ASP primary/secondary configuration is selected using [ASP_PRIMARY](#).

The ASP operation as a primary or secondary interface with MCLK as the clocking source is illustrated in Fig. 4-3 and Fig. 4-4.

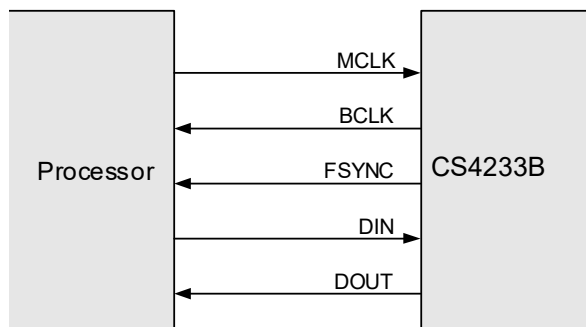


Figure 4-3. Primary Mode, MCLK Clocking Source

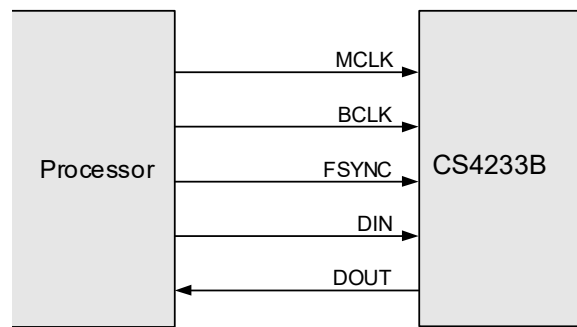


Figure 4-4. Secondary Mode, MCLK Clocking Source

The ASP operation as a primary or secondary interface with a crystal as the clocking source is illustrated in Fig. 4-5 and Fig. 4-6.

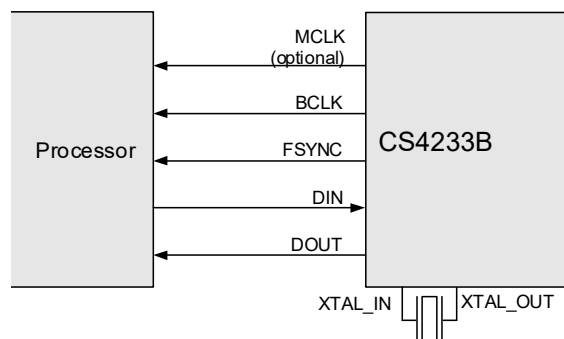


Figure 4-5. Primary Mode, XTAL Clocking Source

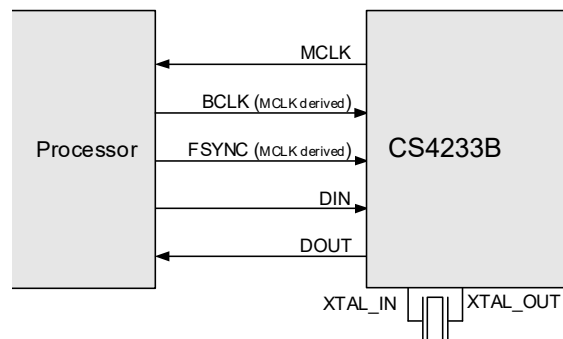


Figure 4-6. Secondary Mode, XTAL Clocking Source

4.8.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-7 through Fig. 4-9. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

I²S Mode data format is shown in Fig. 4-7.

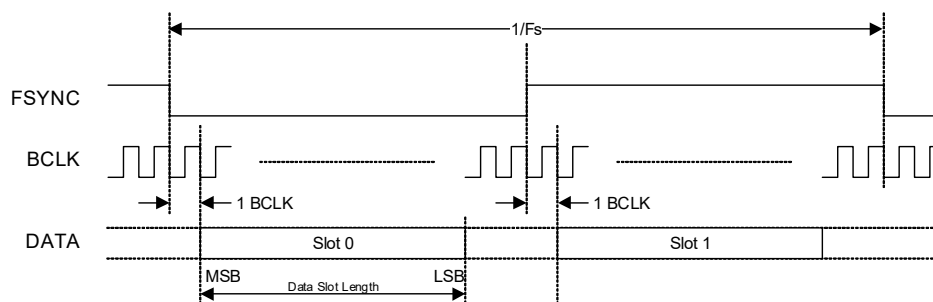


Figure 4-7. I²S Data Format

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

Left-Justified Mode data format is shown in [Fig. 4-8](#).

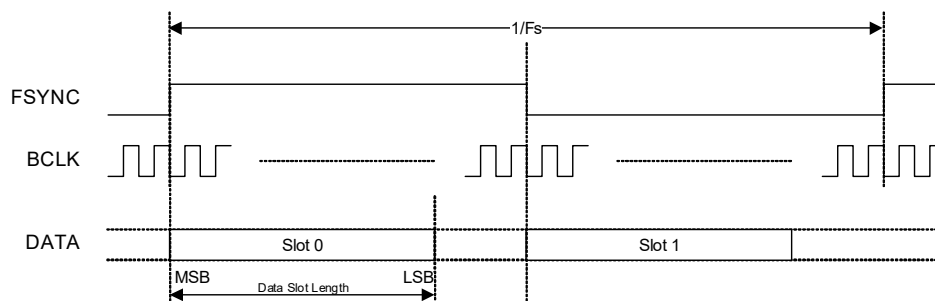


Figure 4-8. Left-Justified Data Format

- In TDM Mode, if the ASP is configured in Secondary Mode, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle. If the ASP is configured in Primary Mode, the FSYNC signal can be configured as a pulse (default) or a square wave (with a 50% duty cycle). If the FSYNC signal is configured as a pulse, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

In ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse, the subsequent channels follow immediately after the first channel. The pulse duration can be anything less than $1/F_s$, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

TDM Mode data format in ASP Secondary Mode and ASP Primary Mode with FSYNC configured as a pulse is shown in [Fig. 4-9](#).

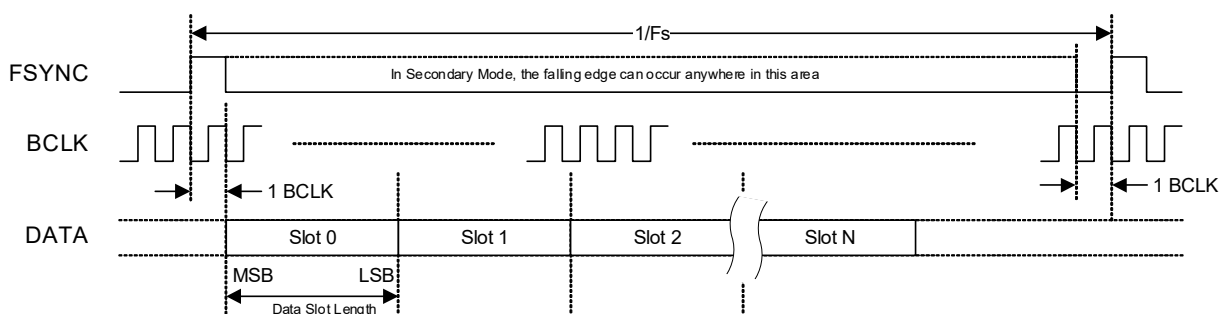


Figure 4-9. TDM Data Format Primary Mode (FSYNC = Pulse) and Secondary Mode

In ASP Primary Mode with the FSYNC signal configured as a square wave, the slots are aligned with both rising and falling edges of FSYNC and half of the available slots occur within each phase of the FSYNC cycle. The total number of available slots is determined by the sample rate, as described in [Table 4-13](#).

- The MSB of the first channel in each phase of the FSYNC cycle is valid on the second BCLK rising edge following the rising and falling FSYNC edge respectively. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, sample rate, and number of available slots, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

TDM Mode data format in ASP Primary Mode with FSYNC configured as a square wave is shown in [Fig. 4-10](#).

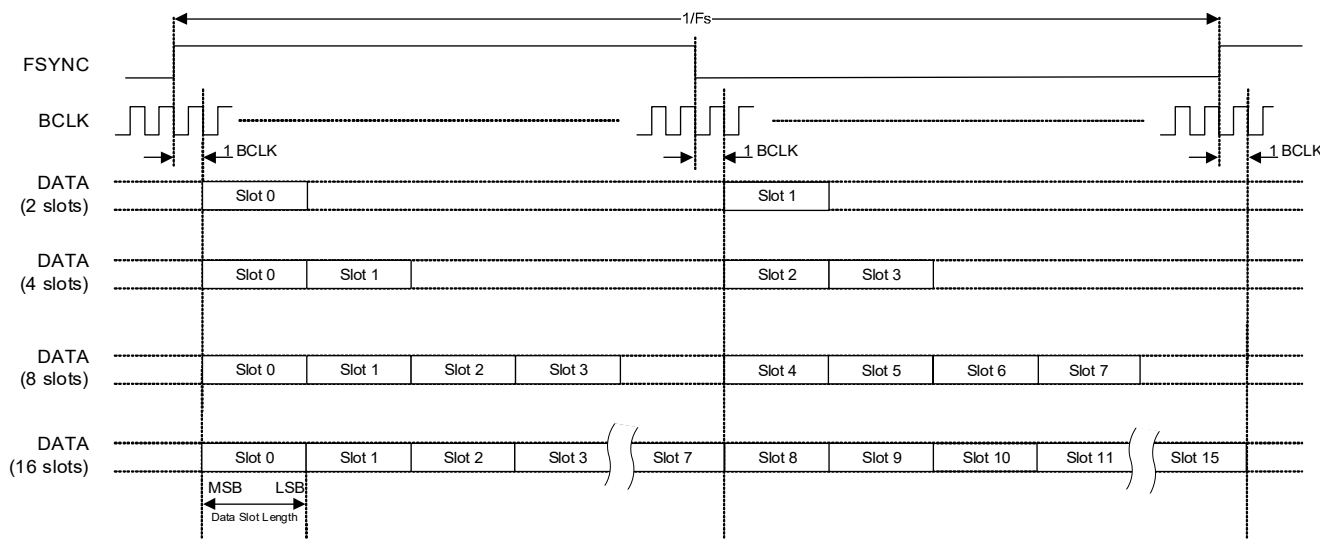


Figure 4-10. TDM Data Format Primary Mode (FSYNC = Square Wave)

4.8.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see [Section 4.2](#)).

In software control mode, the ASP data format is configured using [SAMPLE_RATE](#), and [ASP_FORMAT](#). If ASP Primary Mode is selected (see [Section 4.8.1](#)), the BCLK frequency is configured using [ASP_BCLK_FREQ](#) and the FSYNC waveform type (pulse or square wave) is configured using [ASP_FSYNC_TYPE](#).

In software control mode, the BCLK polarity is selected using [ASP_BCLK_INV](#). The polarity selection is valid in Primary and Secondary Modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in [Fig. 4-11](#) and [Fig. 4-12](#). In hardware control mode, the BCLK polarity is assumed to be noninverted.

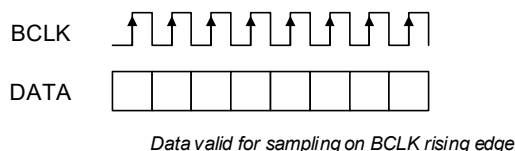


Figure 4-11. Noninverted BCLK

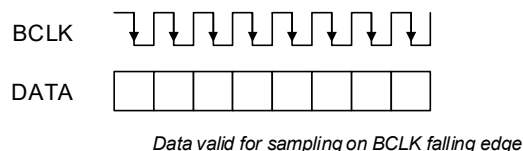


Figure 4-12. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum slots. The ASP data format is configured to support two slots. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 128 BCLK cycles per audio sample at a minimum sample rate of 64 Fs.

- **TDM Mode**—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for sample rates of 44.1, 88.2, 176.4, and 352.8 kHz, or 24.576 MHz for sample rates of 16, 32, 48, 96, 192, and 384 kHz), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

If the ASP is configured for TDM Mode with maximum time slots, the output data (DOUT) can be driven either on the rising or falling BCLK edge. Driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS4233B and the sampling edge at the receiving device.

Note that the ASP timing options are dependent on the behavior of the receiving device. It is assumed, for noninverted BCLK, the data is sampled on the rising BCLK edge. Similarly, for inverted BCLK, it is assumed the data is sampled on the falling BCLK edge.

The DOUT drive options for half-cycle and full-cycle mode are described in [Table 4-12](#). In full-cycle mode, the output data is driven on the same BCLK edge as it is sampled (i.e., one full BCLK cycle before the sampling edge). In half-cycle mode, the output data is driven on the opposite BCLK edge as it is sampled (i.e. one half BCLK cycle before the sampling edge), this is also illustrated in [Table 3-14](#).

Table 4-12. TDM Mode (Maximum Time Slots)—DOUT Drive Timing

TDM Mode ¹	BCLK Polarity ²	DOUT Launching (Drive) Edge	DOUT Latching (Sampling) Edge
Half-cycle	Noninverted	BCLK falling	BCLK rising
	Inverted	BCLK rising	BCLK falling
Full-cycle	Noninverted	BCLK rising	BCLK rising
	Inverted	BCLK falling	BCLK falling

1. The TDM variant is selected using the CONFIG2 pin (in hardware control mode) or [ASP_FORMAT](#) (in software control mode).

2. The BCLK polarity is selected using [ASP_BCLK_INV](#) in software control mode. In hardware control mode, the polarity is assumed noninverted.

The ASP configuration depends on the sample rate and the selected data format as described in [Table 4-13](#).

Table 4-13. ASP Data Format

ASP Format ¹	ASP Sample Rate ^{2,3}	Time Slots per Frame ⁴	BCLK Rate ^{5,6}
I2S, Left-Justified	16 kHz	2	$BCLK \geq 64 \times Fs^{[7]}$
	32 kHz		$BCLK \geq 64 \times Fs^{[8]}$
	44.1 kHz, 48 kHz		$BCLK \geq 64 \times Fs$
	88.2 kHz, 96 kHz		$BCLK \geq 64 \times Fs$
	176.4 kHz, 192 kHz		$BCLK \geq 64 \times Fs$
	352.8 kHz, 384 kHz		$BCLK \geq 64 \times Fs$
	Autodetect (16 kHz–192 kHz)		$BCLK \geq 64 \times Fs$
			$BCLK \geq 64 \times Fs$
TDM—minimum time slots	16 kHz		$BCLK \geq 64 \times Fs^{[7]}$
	32 kHz		$BCLK \geq 64 \times Fs^{[8]}$
	44.1 kHz, 48 kHz		$BCLK \geq 64 \times Fs$
	88.2 kHz, 96 kHz		$BCLK \geq 64 \times Fs$
	176.4 kHz, 192 kHz		$BCLK \geq 64 \times Fs$
	352.8 kHz, 384 kHz		$BCLK \geq 64 \times Fs$
	Autodetect (16 kHz–192 kHz)		$BCLK \geq 64 \times Fs$
			$BCLK \geq 64 \times Fs$
TDM—maximum time slots	16 kHz	16	$BCLK \geq 512 \times Fs^{[7]}$
	32 kHz		$BCLK \geq 512 \times Fs^{[8]}$
	44.1 kHz, 48 kHz		$BCLK = 512 \times Fs$
	88.2 kHz, 96 kHz	8	$BCLK = 256 \times Fs$
	176.4 kHz, 192 kHz	4	$BCLK = 128 \times Fs$
	352.8 kHz, 384 kHz	2	$BCLK = 64 \times Fs$
	Autodetect (16 kHz–192 kHz)	4	$BCLK \geq 128 \times Fs$

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or [ASP_FORMAT](#) (in software control mode).

2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or [SAMPLE_RATE](#) (in software control mode).

3. Sample rates 16 kHz–192 kHz are supported in hardware and software control modes; sample rate 384 kHz is supported in software control mode only.

4. Time slots per frame is the number of data-sample time slots supported on the DIN/DOUT pins.
5. The BCLK rate must be a constant integer multiple of the sample rate (F_s).
6. In ASP Primary Mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP Primary Mode (software control), the BCLK frequency is configured using [ASP_BCLK_FREQ](#).
7. In ASP Primary Mode, the specified minimum BCLK frequency for 16 kHz sample rate is not supported. The available options correspond to $192 \times F_s$, $384 \times F_s$, $768 \times F_s$, or $1536 \times F_s$.
8. In ASP Primary Mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to $96 \times F_s$, $192 \times F_s$, $384 \times F_s$, or $768 \times F_s$.

The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in [Fig. 4-13](#) through [Fig. 4-16](#). Refer to [Table 4-13](#) for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–2 as shown in [Fig. 4-13](#). The minimum BCLK rate is $64 \times F_s$ (where F_s is the sample rate). In ASP Primary Mode, the minimum BCLK rate of $64 \times F_s$ is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

The input data is provided on ASP_DIN; the output data is provided on ASP_DOUT.

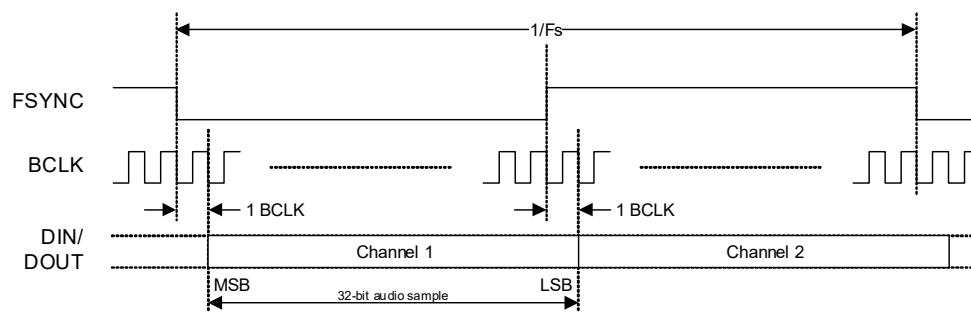


Figure 4-13. I²S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in [Fig. 4-14](#). The minimum BCLK rate is $64 \times F_s$ (where F_s is the sample rate). In ASP Primary Mode, the minimum BCLK rate of $64 \times F_s$ is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

The input data is provided on ASP_DIN; the output data is provided on ASP_DOUT.

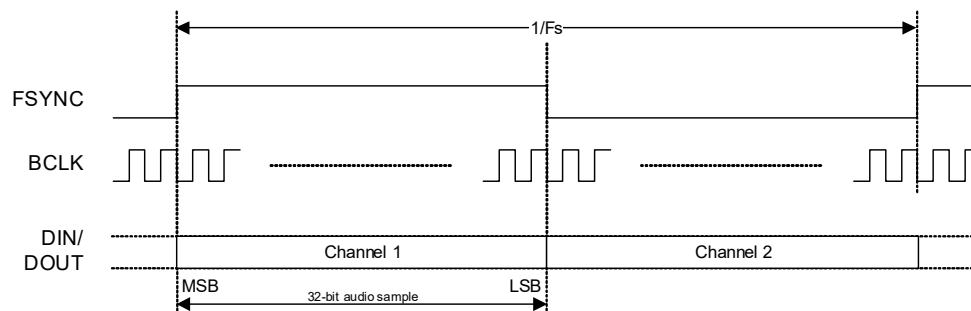


Figure 4-14. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 2, 4, 8, or 16 slots as specified in [Table 4-13](#). In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see [Section 4.2](#)) or else using [ASP_TDM_SLOT](#) (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

The BCLK rate is related to the sample rate (F_s) as described in [Table 4-13](#). Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

The ASP_DOUT pin is high impedance if the CS4233B is not transmitting data, allowing other devices on the bus to transmit data during any unused time slots.

The input data is provided on ASP_DIN; the output data is provided on ASP_DOUT.

An example of the 4-slot TDM format in ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse is shown in Fig. 4-15. In this example, audio channels 1–2 occupy TDM slots 0–1 respectively.

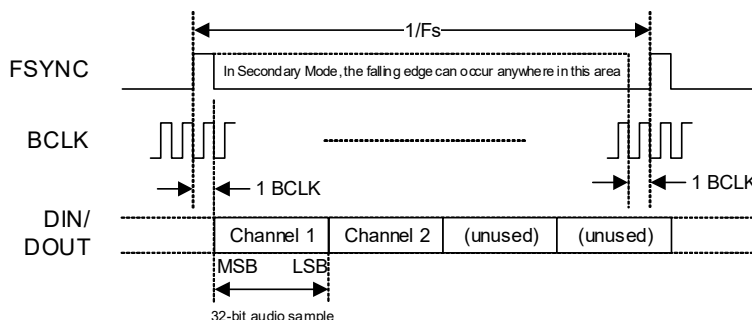


Figure 4-15. TDM Data Format, 4-Slot Example (FSYNC = Pulse)

An example of the 4-slot TDM format in ASP Primary Mode with the FSYNC signal configured as a square wave is shown in Fig. 4-16. In this example, audio channels 0 and 1 occupy TDM slots 0 and 1 in the high (Logic 1) phase of the FSYNC signal, TDM slot 0 and 1 in the low (Logic 0) phase of the FSYNC signal are unused.

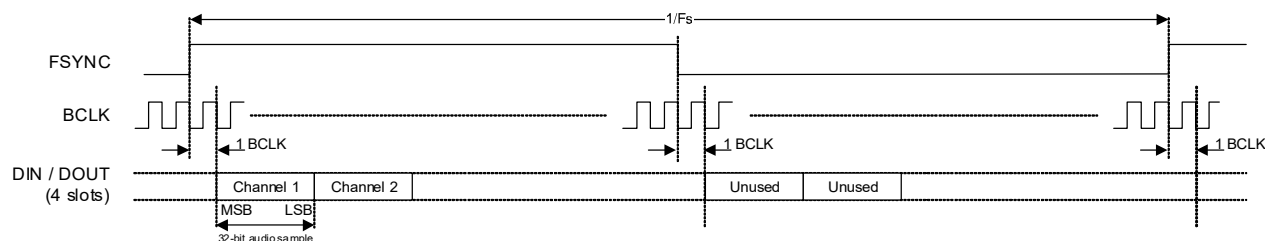


Figure 4-16. TDM Data Format, 4-Slot Example (FSYNC = Square Wave)

4.9 I²C/SPI Control Port

The CS4233B incorporates a control port, supporting I²C or SPI modes of operation; this is selected using CONFIG1, as described in Table 4-1. If the SPI control interface is required, it is recommended to use a pull-up resistor of 100 kΩ. In software control mode, the CS4233B is configured by writing to control registers using the control port.

The control port is automatically configured in I²C mode or SPI mode following the first valid I²C/SPI activity detected after power-on or hardware reset.

4.9.1 I²C Control Port

The I²C control port is supported using the following pins, which must be configured for the I²C function if required:

- CONFIG2/SPI_SDI/I²C_SDA
- CONFIG3/SPI_SDO/I²C_SCL

The CS4233B is a target device on the I²C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS4233B transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS4233B). The LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I²C device address is configured using the CONFIG1 pin as described in [Table 4-14](#).

Table 4-14. I²C Address Selection—CONFIG1 pin

Pin Configuration		I ² C Address
Pull-up to VDD_IO1	0 kΩ	0x46 (write), 0x47 (read)
	4.7 kΩ	0x44 (write), 0x45 (read)
	22 kΩ	0x42 (write), 0x43 (read)
	100 kΩ	0x40 (write), 0x41 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS4233B responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS4233B, the CS4233B responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS4233B returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS4233B, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS4233B returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

The I²C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). The full I²C message protocol also includes a device address, a read/write bit, and other signaling bits (see [Fig. 4-17](#) and [Fig. 4-18](#)).

The CS4233B supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4233B automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

The I²C protocol for a single, 16-bit register write operation is shown in [Fig. 4-17](#).

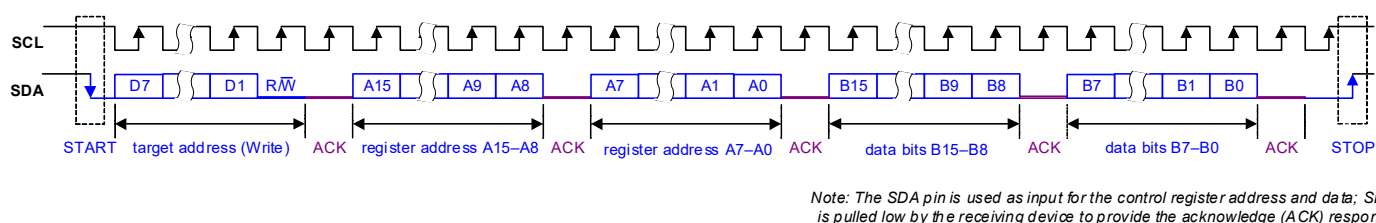


Figure 4-17. Control Interface I²C Register Write

The I²C protocol for a single, 16-bit register read operation is shown in Fig. 4-18.

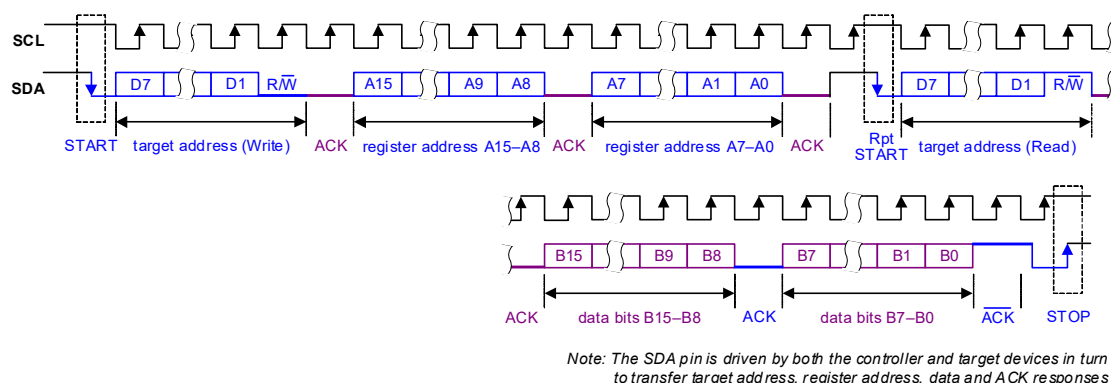


Figure 4-18. Control Interface I²C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-19 through Fig. 4-22. The terminology used in the following figures is detailed in Table 4-15.

Table 4-15. Control Interface (I²C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\bar{A}$	No Acknowledge (SDA high)
P	Stop condition
R/ $\bar{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS4233B
[Gray field]	Data from CS4233B to bus controller

Fig. 4-19 shows a single register write to a specified address.

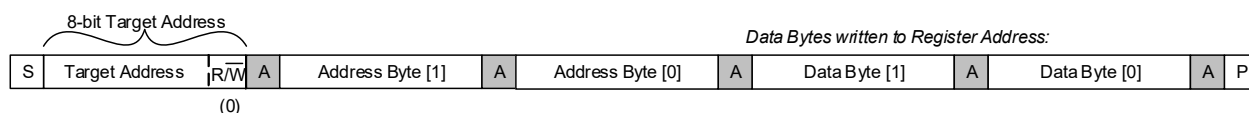


Figure 4-19. Single-Register Write to Specified Address

Fig. 4-20 shows a single register read from a specified address.

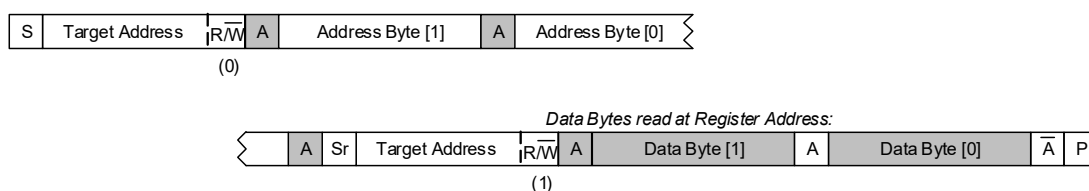


Figure 4-20. Single-Register Read from Specified Address

Fig. 4-21 shows a multiple register write to a specified address.

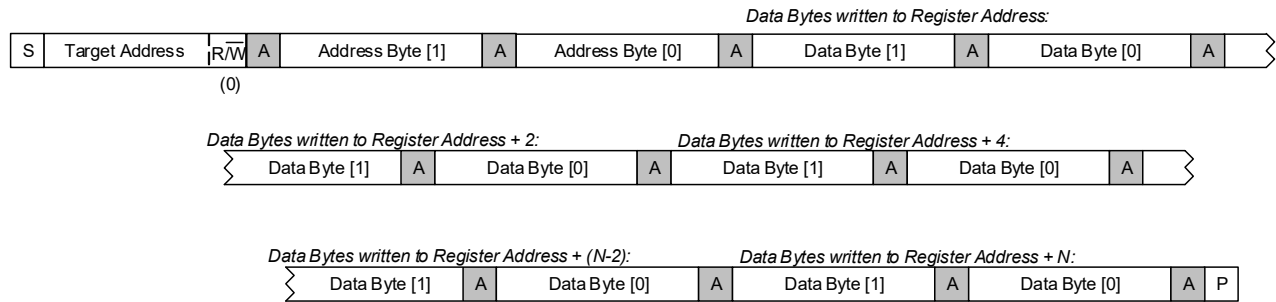


Figure 4-21. Multiple-Register Write to Specified Address

Fig. 4-22 shows a multiple register read from a specified address.

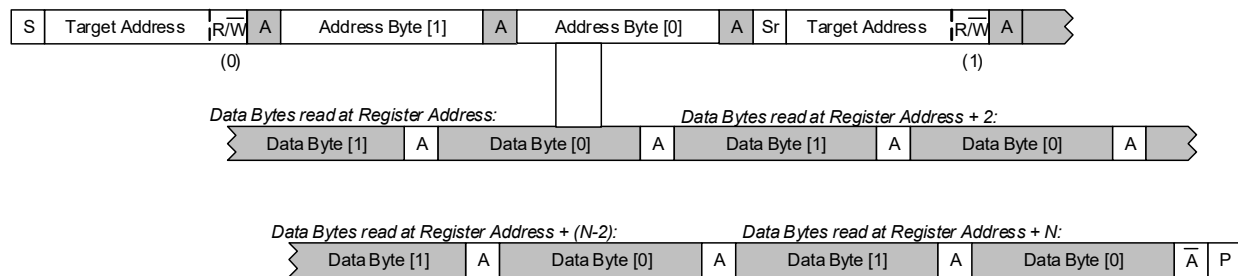


Figure 4-22. Multiple-Register Read from Specified Address

4.9.2 SPI Interface

The SPI interface is supported using the following pins, which must be configured for the SPI function if required:

- CONFIG1/SPI_CS
- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL
- SPI_SCK

To ensure that the control port is inactive prior to use, $\overline{\text{SPI_CS}}$ must be deasserted (i.e., Logic 1) during device startup; RESET must remain asserted (i.e., Logic 0) until SPI_CS is deasserted (i.e., Logic 1), timing information is provided in Table 3-13.

The SDI (data-input) pin supports the following behavior:

- In write operations ($\text{R}/\overline{\text{W}} = 0$), the SDI pin input is driven by the controlling device.
- In read operations ($\text{R}/\overline{\text{W}} = 1$), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-16 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. The full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-23 and Fig. 4-24).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4233B automatically increments the register address at the end of each data word, for as long as $\overline{\text{CS}}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-23 and Fig. 4-24.

Fig. 4-23 shows a single register write to a specified address.

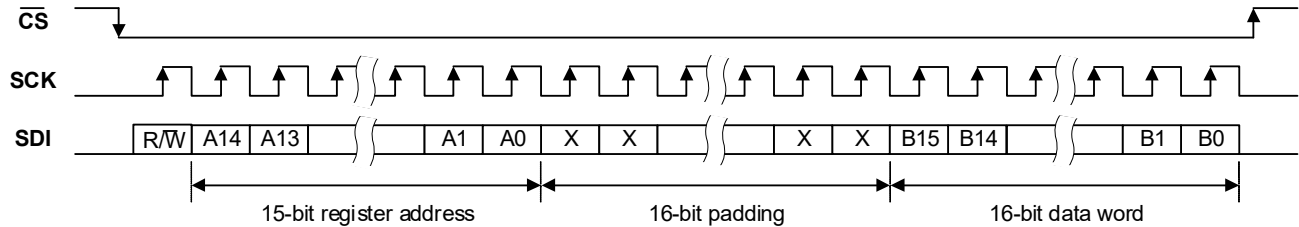


Figure 4-23. Control Interface SPI Register Write

Fig. 4-24 shows a single register read from a specified address.

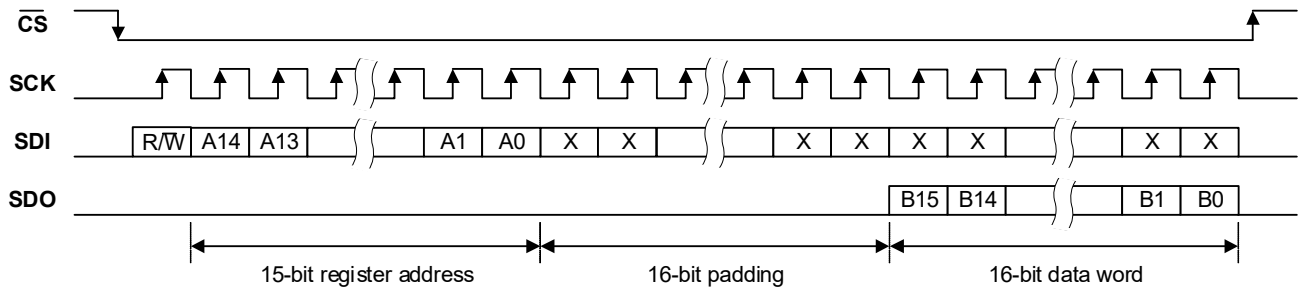


Figure 4-24. Control Interface SPI Register Read

Fig. 4-25 shows a multiple register write to a specified address.

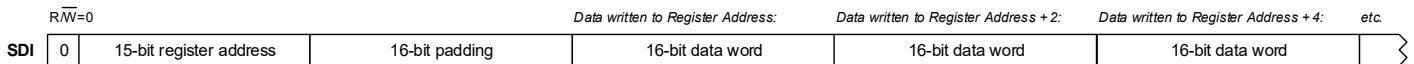


Figure 4-25. Multiple-Register Write to Specified Address

Fig. 4-26 shows a multiple register read from a specified address.

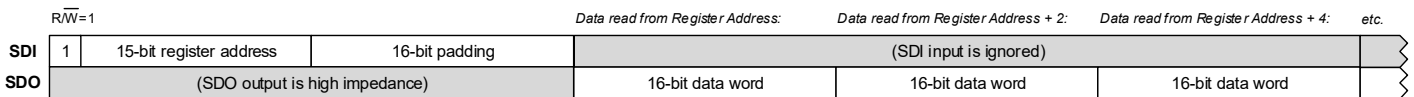


Figure 4-26. Multiple-Register Read from Specified Address

4.10 Interrupts

The CS4233B incorporates an interrupt controller for monitoring event conditions. Inputs to the interrupt controller include clip warning and virtual PAD warning/error conditions.

Any of these input conditions can be used to assert the IRQ output signal. The IRQ signal can be configured as an output on different pins, as described in [Table 4-16](#).

Table 4-16. IRQ Event Logic Output Pins

Pin Name	Power Supply	Control Field	Notes
GPIO1 ¹	VDD_IO2	GPIO1_IRQ_EN	IRQ not supported if pin is configured for virtual PAD.
GPIO2 ¹	VDD_IO2	GPIO2_IRQ_EN	IRQ not supported if pin is configured for virtual PAD.
CONFIG4/CH_IDLE	VDD_IO1	CONFIG4_IRQ_EN	If pin is configured for signal-activity detection, this pin should not be used for IRQ.
SPI_SCK	VDD_IO1	SPI_SCK_IRQ_EN	IRQ not supported if SPI control interface is used.

1. The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see [Table 3-11](#) for details).

An interrupt register bit, [x_INT](#), is associated with each interrupt input, indicating that the respective event has been detected. The interrupt bits are latching fields which, once set, remain set until a 1 is written to the respective bits. The interrupt register bits can be polled at any time or in response to the IRQ output signal being asserted.

A status bit, [x_STS](#), is provided to indicate the current status of the clip warning and virtual PAD inputs.

Mask bits, [x_MASK](#), are provided for each input condition, to enable or disable the respective functions from contributing to the interrupt logic output. The interrupt register bits ([x_INT](#)) remain valid—even if masked—but the masked interrupts do not cause the interrupt logic output to be asserted.

The output can be either CMOS driven or open drain; this is selected using [IRQ_OP_CFG](#).

- If the output is configured as CMOS driven, the IRQ output signal is active high, i.e., Logic 1 if one or more unmasked interrupt is asserted.
- If the output is configured as open drain, the IRQ output signal is active low, i.e., Logic 0 if one or more unmasked interrupt is asserted.

The IRQ signal represents the logical OR of the unmasked interrupt registers. The IRQ output remains asserted until all of the associated interrupts have been either masked or reset.

The IRQ status is indicated using [IRQ_STS](#); this bit is set if one or more unmasked interrupt is asserted.

4.11 Device ID

The device ID, and other associated data, can be read from the control fields listed in [Table 4-17](#).

Table 4-17. Device ID

Label	Description
DEVID_0	Lower bytes of the Device ID
DEVID_1	Upper bytes of the Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Applications

5.1 Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit comprising a high-pass filter and anti-alias filter is shown in Fig. 5-1. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a $2 V_{\text{RMS}}$ differential input.

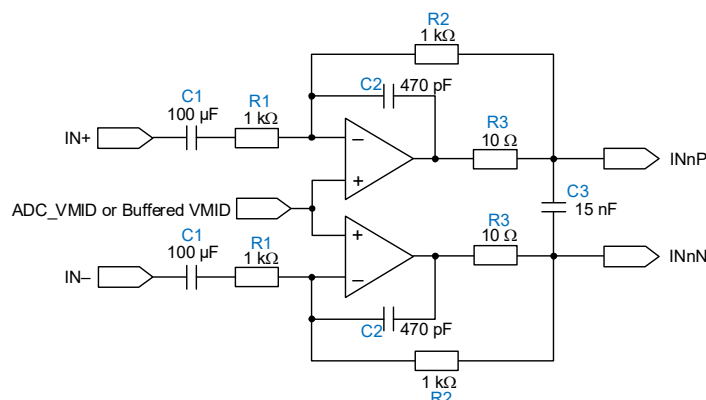


Figure 5-1. Differential Input Buffer Circuit

The high-pass filter is provided by the AC-coupling capacitor, C1 and series resistor, R1. Using the values shown, the -3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1000 \times (100 \times 10^{-6})} = 1.59 \text{ Hz}$$

The anti-alias filter is provided by the operational amplifier and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides an approximated -3 dB cut-off frequency of 424 kHz, suitable for the highest CS4233B sample rate of 384 kHz. The attenuation slope of -12 dB/octave results in 48 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The -3 dB cut-off frequency is approximated by the following equation:

$$F_C = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi \sqrt{1000 \times 10 \times 470 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 424 \text{ kHz}$$

The gain of the input buffer is set by R1 and R2. The gain should be configured to provide a full-scale signal of $2 V_{\text{RMS}}$ at the input to the CS4233B. The values shown in Fig. 5-1 provide a ratio of 1; in this configuration, the buffer supports a full-scale input of $2 V_{\text{RMS}}$.

The ADC_VMID reference is provided as an output from the CS4233B. The ADC_VMID current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current specified in Table 3-12. If a larger current is required, an external VMID buffer should be used; an example of a buffered VMID circuit is provided in Table 3-12.

5.1.1 Unused Input Pins

The recommended input buffer circuit (see Fig. 5-1) provides a differential connection to the input pins INnP and INnN. Alternative input-buffer circuits may use only a single-ended connection to INnP or INnN. If a single-ended input configuration is used, the unused input pin must be connected to a buffered VMID reference, see Table 3-12 for a buffered VMID circuit. If one, or more, input channel is not used (disabled), the respective unused input pin INnP or INnN should be floating (no connection).

5.2 Output Buffer Circuit

The CS4233B incorporates a high-performance sigma-delta current-mode DAC with integrated operational amplifiers for current-to-voltage conversion. External components for the current-to-voltage conversion and out-of-band filtering can be selected for flexible integration and to optimize dynamic range.

5.2.1 Typical Output Circuit

A typical output connection circuit is shown in Fig. 5-2. The circuit produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

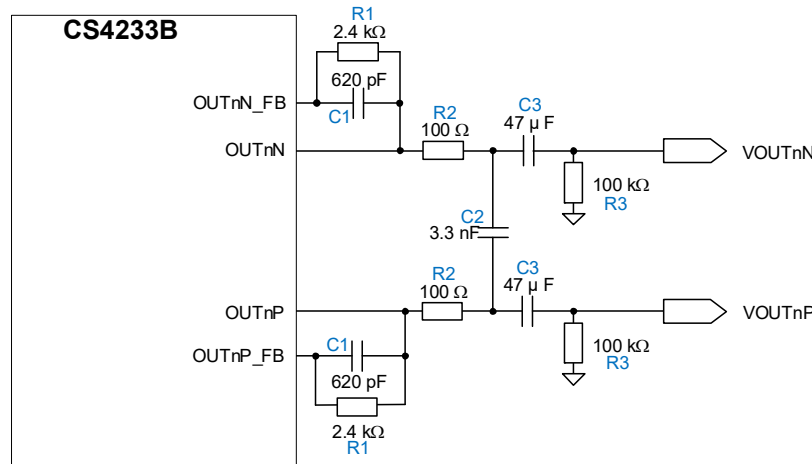


Figure 5-2. Typical Output Connection Circuit

The feedback resistor, R1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTnN and OUTnP pins. R1 is calculated as follows:

$$R_1 = \frac{\text{Full-scale Output Voltage (V}_{\text{RMS}})}{0.835 \text{ mA}_{\text{RMS}}} = \frac{2}{0.835 \times 10^{-3}} = 2.4 \text{ k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107 \text{ kHz}$$

R2 and C2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \times 100 \times (2 \times 3.3 \times 10^{-9})} = 241 \text{ kHz}$$

R3 and C3 form a high-pass filter, which removes the DC bias of the voltage output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_3} = \frac{1}{2\pi \times 100 \times 10^3 \times 47 \times 10^{-6}} = 0.033 \text{ Hz}$$

Note: The cut-off frequency of the filter varies with the load on VOUTnN and VOUTnP.

5.2.2 Alternative Output Circuits

The typical circuit shown in Fig. 5-2 is recommended for optimal performance. Example line driver circuits, designed for high-quality listening experience, are described in Section 5.2.2.1 and Section 5.2.2.2; specifications detailed in Section 3 are not applicable.

5.2.2.1 Example Active Differential Line Driver Circuit

An example of an active differential line-driver circuit is shown in Fig. 5-3, the output connection circuit shown produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

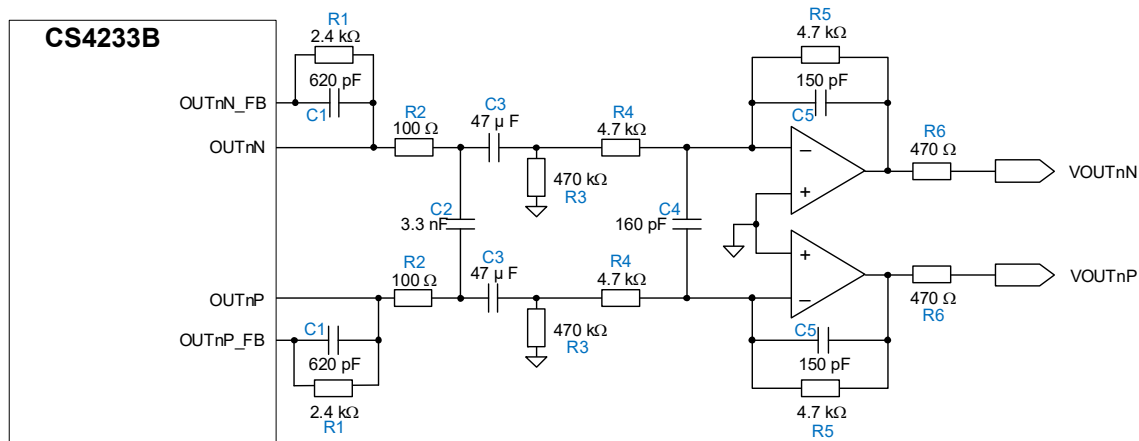


Figure 5-3. Example Active Differential Line Driver Circuit

The feedback resistor, R1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTnN and OUTnP pins. R1 is calculated as follows

$$R_1 = \frac{\text{Full-scale Output Voltage (V}_{\text{RMS}})}{0.835 \text{ mA}_{\text{RMS}}} = \frac{2}{0.835 \times 10^{-3}} = 2.4 \text{ k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107 \text{ kHz}$$

R2 and C2 create an output filter to reduce the out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \times 100 \times (2 \times 3.3 \times 10^{-9})} = 241 \text{ kHz}$$

C3 removes the DC bias of the CS4233B output and forms a high-pass filter with the parallel resistance of R3 and R4. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi \left(\frac{R3 \times R4}{R3 + R4} \right) C_3} = \frac{1}{2\pi \times \left(\frac{470 \times 10^3 \times 4.7 \times 10^3}{470 \times 10^3 + 4.7 \times 10^3} \right) \times 47 \times 10^{-6}} = 0.728 \text{ Hz}$$

R4 and C4 create a low-pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 C_4} = \frac{1}{2\pi \times 4.7 \times 10^3 \times (2 \times 160 \times 10^{-12})} = 105.8 \text{ kHz}$$

R5 and C5 create a low-pass filter within the operational amplifier feedback loop. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_5 C_5} = \frac{1}{2\pi \times 4.7 \times 10^3 \times 150 \times 10^{-12}} = 225.7 \text{ kHz}$$

The gain of the output buffer is set by R4 and R5:

$$\text{Gain} = \frac{R_5}{R_4} = \frac{4.7 \times 10^3}{4.7 \times 10^3} = 1$$

R6 limits the output current; this ensures stability of the output for line-level loads.

5.2.2.2 Example Active Differential-to-Single-Ended Headphone Driver Circuit

An example of an active differential-to-single-ended output circuit is shown in Fig. 5-4. The circuit produces a 2 V_{RMS} single-ended output from a full-scale (0 dBFS) digital input.

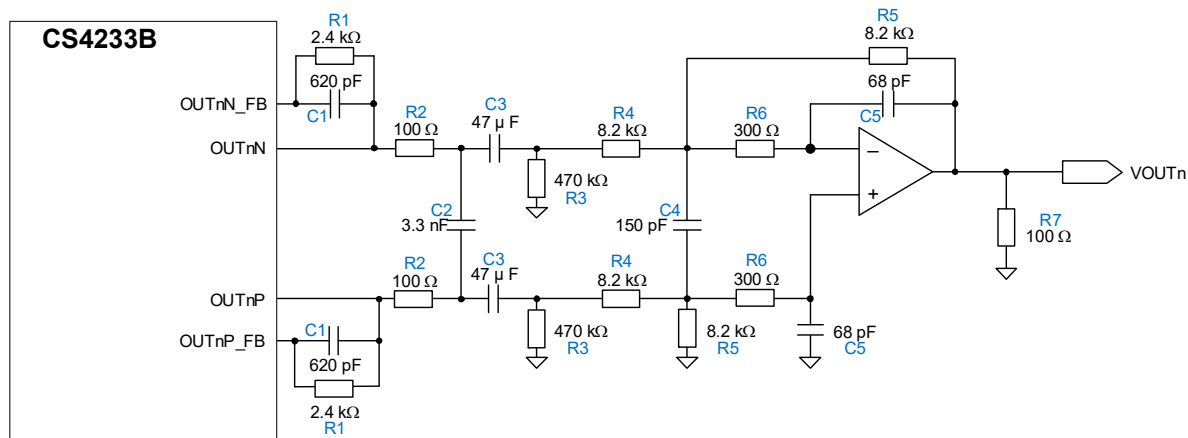


Figure 5-4. Example Differential-to-Single-Ended Output Circuit

The feedback resistor, R1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTnN and OUTnP pins. R1 is calculated as follows:

$$R_1 = \frac{\text{Full-scale Output Voltage (V}_{\text{RMS}})}{0.835 \text{ mA}_{\text{RMS}}} = \frac{2}{0.835 \times 10^{-3}} = 2.4 \text{ k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107 \text{ kHz}$$

R2 and C2 create an output filter to reduce the out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \times 100 \times (2 \times 3.3 \times 10^{-9})} = 241 \text{ kHz}$$

C3 removes the DC bias of the CS4233B output and forms a high-pass filter with parallel resistance of R3 and R4. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi \left(\frac{R_3 \times R_4}{R_3 + R_4} \right) C_3} = \frac{1}{2\pi \times \left(\frac{470 \times 10^3 \times 8.2 \times 10^3}{470 \times 10^3 + 8.2 \times 10^3} \right) \times 47 \times 10^{-6}} = 0.42 \text{ Hz}$$

R4 and C4 create a low-pass filter. The cut-off frequency of the low-pass filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 C_4} = \frac{1}{2\pi \times (8.2 \times 10^3) \times (2 \times 150 \times 10^{-12})} = 64.7 \text{ kHz}$$

R5, R6, and C5 create a low-pass filter within the operational amplifier feedback loop. The cut-off frequency of the low-pass filter is calculated as follows:

$$F_C = \frac{1}{2\pi (R_5 + R_6) C_5} = \frac{1}{2\pi (8.2 \times 10^3 + 300) \times 68 \times 10^{-12}} = 275.4 \text{ kHz}$$

The gain of the output buffer is set by R4 and R5:

$$\text{Gain} = \frac{R_5}{R_4} = \frac{8.2 \times 10^3}{8.2 \times 10^3} = 1$$

R7 limits the output current and ensures stability of the circuit for headphone-to-line-level loads.

5.2.3 Unused Output Pins

The typical output connection circuit (Fig. 5-2) provides a differential output. Alternative output buffer circuits may only provide a single-ended output configuration. In this case, or where an output channel is not used, any unused output pin (OUTnX) must be connected to its respective OUTnX_FB pin, as illustrated in Fig. 5-5.

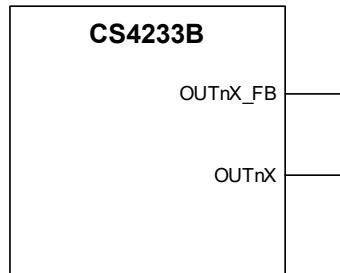


Figure 5-5. Unused Output Pin Connection

5.3 PCB Layout Guidelines

The recommended layout guidelines are provided in this section. Typical external components are described in [Section 2](#).

5.3.1 General Layout Guidelines

The following general guidelines should be followed:

- Digital signals should be supported using a controlled 50 Ω characteristic impedance.
- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analog and digital signals next to each other.
- If a signal crosses another signal on an adjacent layer, they should cross perpendicularly to prevent coupling.
- Signals must not cross power-plane shapes or ground cut-offs on an adjacent layer.

5.3.2 Component Placement

The following guidelines on component placement should be followed:

- Power supply decoupling capacitors should be placed as close as possible to the CS4233B, with a strong connection to the ground plane.
- The voltage reference (ADC_VMID and DAC_VMID) capacitors and LDO filter (LDO_VD_FILT) capacitor should be placed close to the CS4233B, with a strong connection to the ground plane.

5.3.3 Ground Routing

The following guidelines are recommended for ground connection:

- The ground paddle of the CS4233B should be connected to the ground plane with at least five vias.
- The ground paddle should not be connected directly to any pin.

5.3.4 VDD_A Routing

The following guidelines are recommended for the VDD_A supply:

- VDD_A1 and VDD_A2 should be star-connected to a 3.3 V power plane.
- Decoupling capacitors (0.01 μ F and 4.7 μ F) should be provided for each supply pin (VDD_A1 and VDD_A2), as shown in [Section 2](#).

5.3.5 DAC_FILT Routing

The following guidelines are recommended for the DAC_FILT_P and DAC_FILT_N pins:

- Decoupling capacitors (22 μ F) should be connected to DAC_FILT_P and DAC_FILT_N, as shown in [Section 2](#).
- The DAC_FILT_P and DAC_FILT_N decoupling capacitors should be placed close to the CS4233B.
- The DAC_FILT_P decoupling capacitor should be connected to VDD_A1 as close as possible to the decoupling capacitors for VDD_A1.
- The DAC_FILT_N decoupling capacitor should be connected to the ground plane with a dedicated via.

5.3.6 ADC_FILT Routing

- Decoupling capacitors (0.1 μ F, 1 μ F, and 100 μ F) should be connected to the ADC_FILT_P and ADC_FILT_N pins, as shown in [Section 2](#).
- The 0.1 μ F capacitor should be placed closest to the CS4233B, then the 1 μ F capacitor, then the 100 μ F capacitor.
- The ADC_FILT_N trace should be connected to ground after the 100 μ F capacitor.
- The ADC_FILT_P trace should be star-connected to VDD_A2 using a 1 Ω resistor placed after the 100 μ F capacitor.

5.4 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise operational amplifiers should be used, such as Texas Instruments OPA1656. The operational amplifiers should meet the minimum performance requirements noted in [Table 5-1](#).

Table 5-1. Op-Amp Specification

Parameter	Specification
Input noise	<5 nV/ $\sqrt{\text{Hz}}$
Unity gain bandwidth	>15 MHz
Slew rate	5 V/ μ s
Total harmonic distortion plus noise (THD+N)	<-128 dB

5.4.1 Crystal Component Selection

The crystal oscillator (see [Section 4.4](#)) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in [Fig. 5-6](#). A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

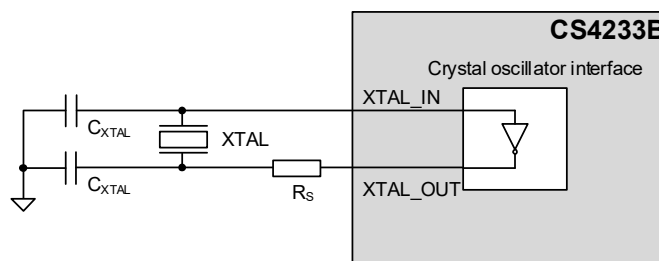


Figure 5-6. Crystal Oscillator Connection

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD_IO2 operating voltage as described in [Table 3-13](#).

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS4233B is compatible with a wide variety of crystal components, including the KC3225Z series of oscillators. Note that for a reference frequency of 45.1584 MHz a custom crystal may be required.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is $2 \times C_L$.
3. **Series resistor.** In the first instance, assume the series resistor R_S is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S , together with the crystal characteristics. If the required gain margin is less than 5, a different crystal selection must be made (Step 1).

The gain margin is calculated as follows:
$$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

where:

Transconductance = transconductance of the crystal interface (S)

ESR = equivalent series resistance (ESR) of the crystal (Ω)

R_S = series resistance (Ω)

f_{XTAL} = resonant frequency of the crystal (Hz)

C_L = load capacitance of the crystal (F)

C_0 = shunt capacitance of the crystal (F)

5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

The drive level (W) is calculated as follows:
$$\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$$

where:

ESR = equivalent series resistance (ESR) of the crystal (Ω)

f_{XTAL} = resonant frequency of the crystal (Hz)

V = Peak voltage across the crystal (V)

C_L = load capacitance of the crystal (F)

C_0 = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in [Fig. 5-7](#).

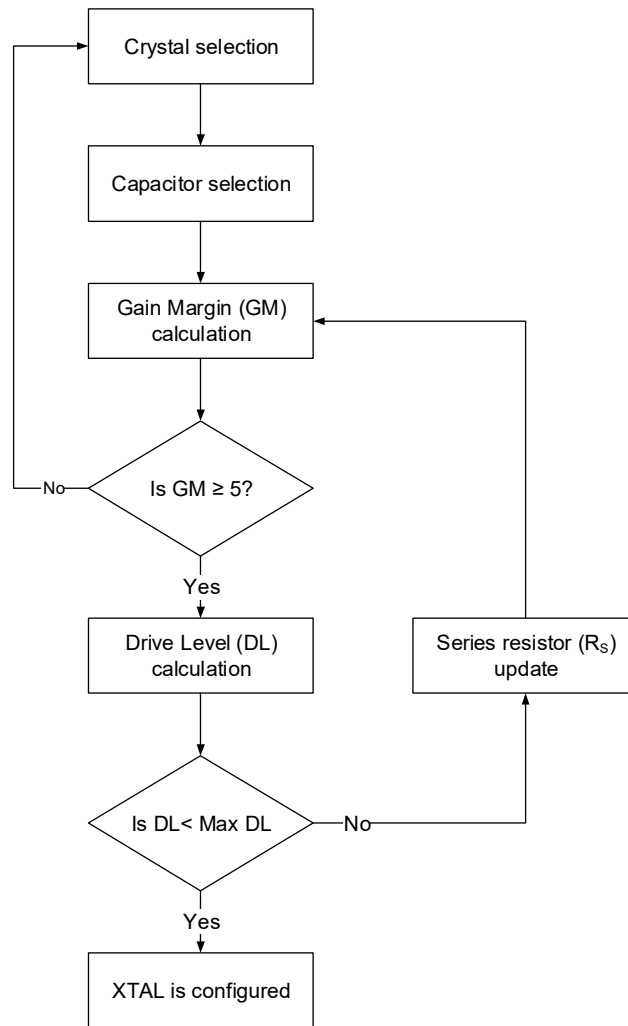


Figure 5-7. Crystal Oscillator Component Selection

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS4233B.

- The register field default values are established upon the deassertion of the **RESET** pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access
 Read-only access
 Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	DEVID	Section 6.1	Section 7.1
0x0000 0040	CONFIG	Section 6.2	Section 7.2
0x0000 0080	INPUT_PATH	Section 6.3	Section 7.3
0x0000 00C0	OUTPUT_PATH	Section 6.4	Section 7.4
0x0000 2000	SIG_CTRL	Section 6.5	Section 7.5
0x0000 3D00	PIN_CONFIG	Section 6.6	Section 7.6
0x0000 3E00	IRQ_CONFIG	Section 6.7	Section 7.7

6.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000 p. 53	DEVID_0	DEVID_0															
		0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0
0x0000 0002 p. 53	DEVID_1	DEVID_1															
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0x0000 0004 p. 53	REVID	—								AREVID				MTLREVID			
		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1
0x0000 0022 p. 54	SW_RESET	SW_RESET								—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040 p. 54	CLK_CFG	—		SYSCLK_FREQ	SYSCLK_SRC	—											
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0042 p. 54	SAMPLE_RATE	—												SAMPLE_RATE			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
0x0000 0044 p. 54	CHIP_ENABLE	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048 p. 55	ASP_CFG	—								ASP_BCLK_INV		ASP_PRIMARY	—			ASP_BCLK_FREQ	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0050	SIGNAL_PATH_CFG	—										ASP_FSYNC_TYPE	ASP_TDM_SLOT		ASP_FORMAT		
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3 INPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0080	IN_ENABLES	—														IN2_ADC_EN	IN1_ADC_EN
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0082	IN_RAMP_SUM	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC			—	IN_RAMP_RATE_INC		
p. 56		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 008A	IN_INV	—														IN2_INV	IN1_INV
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0090	IN1_VOL_CTRL	IN1_MUTE	—						IN1_VOL								
p. 56		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0092	IN2_VOL_CTRL	IN2_MUTE	—						IN2_VOL								
p. 57		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00A0	IN_VOL_UPDATE	—															IN_VU
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4 OUTPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00C0	OUT_ENABLES	—								OUT_LOAD_CFG	—					OUT2_DAC_EN	OUT1_DAC_EN
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C2	OUT_RAMP_SUM	—								OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC			
p. 58		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 00C4	OUT_DEEMPH	—														OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00CA	OUT_INV	—														OUT2_INV	OUT1_INV
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x0000 00D0	OUT1_VOL_CTRL	OUT1_MUTE	—						OUT1_VOL								
p. 59		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D2	OUT2_VOL_CTRL	OUT2_MUTE	—						OUT2_VOL								
p. 59		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E0	OUT_VOL_UPDATE	—															OUT_VU
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E4	SHUTDOWN_CTRL1	—															DAC_SHUTDO WN
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.5 SIG_CTRL

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 200C p. 60	IO_CTRL	—					DB_TIME			—		SW TYPE	—				
		0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
0x0000 2010 p. 60	GPIO_STS	—				GPO_STS				—				GPI_STS			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2110 p. 60	IN_EMA_EN	—			IN_EMA_TIME					—						IN2 EMA_EN	IN1 EMA_EN
		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0x0000 2140 p. 61	IN_PAD_CFG	—						IN2 PAD_LD_ EN	IN1 PAD_LD_ EN	—						IN2_ PAD_ AUTO_ EN	IN1_ PAD_ AUTO_ EN
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2142 p. 61	IN_PAD_SIGNAL	IN_PAD LD_AVG	—										IN_PAD_LD_TIME				
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0x0000 2146 p. 61	IN1_PAD_THR	—				IN1_PAD_LOW_THR				—			IN1_PAD_HIGH_THR				
		0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1
0x0000 214A p. 62	IN2_PAD_THR	—				IN2_PAD_LOW_THR				—			IN2_PAD_HIGH_THR				
		0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1
0x0000 2170 p. 62	IN_SIG_ACT_EN	—															IN_SIG_ACT_EN
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2176 p. 62	IN1_SIG_ACT_THR	—				IN1_SIG_ACT_HIGH_THR				—			IN1_SIG_ACT_LOW_THR				
		0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1
0x0000 217A p. 63	IN2_SIG_ACT_THR	—				IN2_SIG_ACT_HIGH_THR				—			IN2_SIG_ACT_LOW_THR				
		0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	1
0x0000 2202 p. 63	IN1_CFG_GPIO	—			IN1_GPI_POL	—	IN1_GPI_SEL			—			IN1_GPO4_SEL	IN1_GPO3_SEL	IN1_GPO2_SEL	IN1_GPO1_SEL	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2206 p. 63	IN2_CFG_GPIO	—			IN2_GPI_POL	—	IN2_GPI_SEL			—			IN2_GPO4_SEL	IN2_GPO3_SEL	IN2_GPO2_SEL	IN2_GPO1_SEL	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2226 p. 64	IN1_INT_GAIN	IN1_UPDATE	—	IN1_INT_ANA_GAIN		—			IN1_INT_DIG_GAIN								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 222E p. 64	IN2_INT_GAIN	IN2_UPDATE	—	IN2_INT_ANA_GAIN		—			IN2_INT_DIG_GAIN								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2262 p. 65	IN1_LOW_GPO	IN1_LOW_GPO4	IN1_LOW_GPO3	IN1_LOW_GPO2	IN1_LOW_GPO1	—											
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2266 p. 65	IN1_LOW_INT_GAIN	IN1_LOW_UPDATE	—	IN1_LOW_INT_ANA_GAIN		—			IN1_LOW_INT_DIG_GAIN								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 226A p. 66	IN2_LOW_GPO	IN2_LOW_GPO4	IN2_LOW_GPO3	IN2_LOW_GPO2	IN2_LOW_GPO1	—											
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 226E p. 66	IN2_LOW_INT_GAIN	IN2_LOW_UPDATE 0	— 0	IN2_LOW_INT_ANA_GAIN 0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22C2 p. 66	IN1_HIGH_GPO	IN1_HIGH_GPO4 0	IN1_HIGH_GPO3 0	IN1_HIGH_GPO2 0	IN1_HIGH_GPO1 0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22C6 p. 67	IN1_HIGH_INT_GAIN	IN1_HIGH_UPDATE 0	— 0	IN1_HIGH_INT_ANA_GAIN 0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22CA p. 67	IN2_HIGH_GPO	IN2_HIGH_GPO4 0	IN2_HIGH_GPO3 0	IN2_HIGH_GPO2 0	IN2_HIGH_GPO1 0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22CE p. 67	IN2_HIGH_INT_GAIN	IN2_HIGH_UPDATE 0	— 0	IN2_HIGH_INT_ANA_GAIN 0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2510 p. 68	OUT_SIG_ACT_EN	0	— 0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0x0000 2514 p. 68	OUT1_SIG_ACT_THR	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
0x0000 2518 p. 68	OUT2_SIG_ACT_THR	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

6.6 PIN_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3D1C p. 69	PAD_IRQ_CFG	IRQ_OP_CFG 0	— 0	0	0	0	0	0	GPIO1_IRQ_EN 0	GPIO2_IRQ_EN 0	— 0	0	CONFIG4_IRQ_EN 0	SPL_SCK_IRQ_EN 0	— 0	0	0

6.7 IRQ_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3E04 p. 69	IRQ_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ_STS 0
0x0000 3E1C p. 69	IRQ_ADC_EVENT_INT	— 0	— 0	— 0	— 0	IN2_PAD_LOW_INT 0	IN1_PAD_LOW_INT 0	IN2_PAD_HIGH_INT 0	IN1_PAD_HIGH_INT 0	GAIN_CONFLICT_INT 0	— 0	— 0	— 0	— 0	IN2_CLIP_WARN_INT 0	IN1_CLIP_WARN_INT 0	— 0
0x0000 3E2C p. 70	IRQ_ADC_EVENT_MASK	— 1	— 1	— 0	— 0	IN2_PAD_LOW_MASK 1	IN1_PAD_LOW_MASK 1	IN2_PAD_HIGH_MASK 1	IN1_PAD_HIGH_MASK 1	GAIN_CONFLICT_MASK 1	— 0	— 0	— 0	— 0	IN2_CLIP_WARN_MASK 0	IN1_CLIP_WARN_MASK 0	— 0
0x0000 3E5C p. 71	IRQ_ADC_EVENT_STS	— 0	— 0	— 0	— 0	IN2_PAD_LOW_STS 0	IN1_PAD_LOW_STS 0	IN2_PAD_HIGH_STS 0	IN1_PAD_HIGH_STS 0	— 0	— 0	— 0	— 0	— 0	IN2_CLIP_WARN_STS 0	IN1_CLIP_WARN_STS 0	— 0

7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS4233B.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:



Read/write access



Read-only access



Write-only access

7.1 DEVID

7.1.1 DEVID_0

Address: 0x0000 0000

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID_0															
Default	0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0

Bits	Name	Description
15:0	DEVID_0	This register indicates the lower bytes of Device ID CS4233B 0x0000–0x2331 = Reserved 0x2332 = (Default) CS4233B 0x2333–0xFFFF = Reserved

7.1.2 DEVID_1

Address: 0x0000 0002

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description
15:0	DEVID_1	This register indicates the upper bytes of Device ID CS4233B 0x0000–0x0003 = Reserved 0x0004 = (Default) CS4233B 0x0005–0xFFFF = Reserved

7.1.3 REVID

Address: 0x0000 0004

RO	15...8	7	6	5	4	3	2	1	0
	—	AREVID				MTLREVID			
Default	0x00	1	0	1	0	0	0	0	1

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0x9 = Reserved 0xA = (Default) Revision Ax 0xB–0xF = Reserved
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = Reserved 0x1 = (Default) Revision x1 0x2–0xF = Reserved

7.1.4 SW_RESET

Address: 0x0000 0022

WO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

7.2 CONFIG

7.2.1 CLK_CFG

Address: 0x0000 0040

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		SYSCLK_FREQ	SYSCLK_SRC	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:14	—	Reserved
13	SYSCLK_FREQ	System clock frequency. 0 = (Default) 24.576/22.5792 MHz 1 = 49.152/45.1584 MHz
12	SYSCLK_SRC	System clock source. If XTAL is selected, the MCLK is the output clock. 0 = (Default) MCLK input 1 = XTAL input
11:0	—	Reserved

7.2.2 SAMPLE_RATE

Address: 0x0000 0042

RW	15...8	7	6	5	4	3	2	1	0
	—	—							SAMPLE_RATE
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 16-192 kHz, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/352.8 kHz 101 = Reserved 110 = Auto-detect 111 = 16 kHz

7.2.3 CHIP_ENABLE

Address: 0x0000 0044

RW	15...8	7	6	5	4	3	2	1	0
	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

7.2.4 ASP_CFG

Address: 0x0000 0048

RW	15...8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—	—	—	ASP_BCLK_FREQ	—
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, DIN data is valid on BCLK rising edge. DOUT data is driven on BCLK falling edge (TDM half-cycle mode) or rising edge (TDM full-cycle mode). In inverted mode, DIN data is valid on BCLK falling edge. DOUT data is driven on BCLK rising edge (TDM half-cycle mode) or falling edge (TDM full-cycle mode). 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 24.576 / 49.152 MHz system clock, or multiples of 2.8224 MHz for 22.5792 / 45.1584 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

7.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15...8	7	6	5	4	3	2	1	0
	—	—	ASP_FSYNC_TYPE	—	ASP_TDM_SLOT	—	—	ASP_FORMAT	—
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_FSYNC_TYPE	Configure ASP_FSYNC as pulse or square wave (50% duty cycle) in TDM mode. Only applicable when ASP is in Primary Mode. 0 = (Default) FSYNC Pulse 1 = FSYNC Square Wave
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. 000 = (Default) Slots 0-1 001 = Slots 2-3 010 = Slots 4-5 011 = Slots 6-7 100 = Slots 8-9 101 = Slots 10-11 110 = Slots 12-13 111 = Slots 14-15
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–100 = Reserved 101 = TDM Mode maximum time slots, full cycle 110 = TDM Mode maximum time slots, half cycle 111 = TDM Mode minimum time slots

7.3 INPUT_PATH

7.3.1 IN_ENABLES

Address: 0x0000 0080

RW	15...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	IN2_ADC_EN	IN1_ADC_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved

Bits	Name	Description
1	IN2_ADC_EN	Channel 2 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled
0	IN1_ADC_EN	Channel 1 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled

7.3.2 IN_RAMP_SUM

Address: 0x0000 0082

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC				—	IN_RAMP_RATE_INC	
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Name	Description
15:12	—	Reserved
11:8	IN_CLIP_THRESH	Input clip-warning threshold. 0x0 = (Default) 0.0 dBFS 0x1 = -0.125 dBFS 0x2 = -0.25 dBFS 0x3 = -0.5 dBFS 0x4 = -1.0 dBFS 0x5 = -3.0 dBFS 0x6 = -6.0 dBFS 0x7-0xF = Reserved
7	—	Reserved
6:4	IN_RAMP_RATE_DEC	ADC input volume Decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	IN_RAMP_RATE_INC	ADC input volume Increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

7.3.3 IN_INV

Address: 0x0000 008A

RW	15...8	7	6	5	4	3	2	1	0
	—	—						IN2_INV	IN1_INV
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	IN2_INV	Channel 2 ADC invert. 0 = (Default) No inversion 1 = ADC data invert
0	IN1_INV	Channel 1 ADC invert. 0 = (Default) No inversion 1 = ADC data invert

7.3.4 IN1_VOL_CTRL

Address: 0x0000 0090

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_MUTE	—							IN1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_MUTE	Channel 1 input mute. 0 = Unmute 1 = (Default) Mute

Bits	Name	Description
14:9	—	Reserved
8:0	IN1_VOL	Channel 1 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps. 0x000 = (Default) 0.0 dB 0x001 = –0.5 dB ... 0x0FF = –127.5 dB 0x100 = Reserved 0x101 = 0.5 dB 0x102 = 1.0 dB ... 0x13C = 30.0 dB 0x13D–0x1FF = Reserved

7.3.5 IN2_VOL_CTRL

Address: 0x0000 0092

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_MUTE	—							IN2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_MUTE	Channel 2 input mute. 0 = Unmute 1 = (Default) Mute
14:9	—	Reserved
8:0	IN2_VOL	Channel 2 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps. 0x000 = (Default) 0.0 dB 0x001 = –0.5 dB ... 0x0FF = –127.5 dB 0x100 = Reserved 0x101 = 0.5 dB 0x102 = 1.0 dB ... 0x13C = 30.0 dB 0x13D–0x1FF = Reserved

7.3.6 IN_VOL_UPDATE

Address: 0x0000 00A0

WO	15...8	7	6	5	4	3	2	1	0
	—	—							IN_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IN_VU	Global ADC input volume update trigger. 0 = (Default) No action 1 = Write 1 to trigger an update of all input volume/mute registers

7.4 OUTPUT_PATH

7.4.1 OUT_ENABLES

Address: 0x0000 00C0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—							OUT_LOAD_CFG	—					OUT2_DAC_EN		OUT1_DAC_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:9	—	Reserved
8	OUT_LOAD_CFG	Output driving configuration. 0 = (Default) 3k load 1 = 10k load
7:2	—	Reserved
1	OUT2_DAC_EN	Channel 2 output enable. 0 = (Default) Disabled 1 = Enabled
0	OUT1_DAC_EN	Channel 1 output enable. 0 = (Default) Disabled 1 = Enabled

Address: 0x0000 00C2

RW	15...8	7	6	5	4	3	2	1	0
	—	—	OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
Default	0x00	0	0	1	0	0	0	1	0

Bits	Name	Description
15:7	—	Reserved
6:4	OUT_RAMP_RATE_DEC	DAC output volume decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	OUT_RAMP_RATE_INC	DAC output volume increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

Address: 0x0000 00C4

RW	15...8	7	6	5	4	3	2	1	0
	—	—						OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OUT_DEEMPH_FILT_SEL	Deemphasis filter sample-rate selection. 0 = (Default) 44.1 kHz 1 = 48.0 kHz
0	OUT_DEEMPH_EN	Deemphasis filter enable. 0 = (Default) Deemphasis disabled 1 = Deemphasis enabled

Address: 0x0000 00CA

RW	15...8	7	6	5	4	3	2	1	0
	—	—						OUT2_INV	OUT1_INV
Default	0x00	0	0	0	0	0	0	1	1

Bits	Name	Description
15:2	—	Reserved
1	OUT2_INV	Channel 2 DAC invert. 0 = No inversion 1 = (Default) DAC data invert
0	OUT1_INV	Channel 1 DAC invert. 0 = No inversion 1 = (Default) DAC data invert

7.4.5 OUT1_VOL_CTRL
Address: 0x0000 00D0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_MUTE	—							OUT1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_MUTE	DAC output Channel 1 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT1_VOL	DAC output Channel 1 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB ... 0xFF = –127.5 dB

7.4.6 OUT2_VOL_CTRL
Address: 0x0000 00D2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_MUTE	—							OUT2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_MUTE	DAC output Channel 2 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT2_VOL	DAC output Channel 2 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB ... 0xFF = –127.5 dB

7.4.7 OUT_VOL_UPDATE
Address: 0x0000 00E0

WO	15...8	7	6	5	4	3	2	1	0
	—	—							OUT_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	OUT_VU	Global output volume update trigger. 0 = (Default) No action 1 = Write 1 to trigger an update of all output volume/mute registers

7.4.8 SHUTDOWN_CTRL1
Address: 0x0000 00E4

RW	15...8	7	6	5	4	3	2	1	0
	—	—							DAC_SHUTDOWN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	DAC_SHUTDOWN	DAC reference shutdown control. Can be used to minimize power consumption if all output paths are disabled. 0 = (Default) Enable DAC reference 1 = Shutdown DAC reference

7.5 SIG_CTRL

7.5.1 IO_CTRL

Address: 0x0000 200C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				DB_TIME				—		SW_TYPE	—				
Default	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	DB_TIME	GPI debounce time, base 32 kHz. 000 = 124 us 100 = 16 ms 001 = 2 ms 101 = 32 ms 010 = 4 ms 110 = 64 ms 011 = (Default) 8 ms 111 = 128 ms
7:6	—	Reserved
5	SW_TYPE	GPI type selection. Select toggle switch for rising-edge detection or latching switch for level detection. 0 = Toggle switch 1 = (Default) Latching switch
4:0	—	Reserved

7.5.2 GPIO_STS

Address: 0x0000 2010

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				GPO_STS				—				GPI_STS			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	GPO_STS	GPO read back status.
7:4	—	Reserved
3:0	GPI_STS	GPI read back status.

7.5.3 IN_EMA_EN

Address: 0x0000 2110

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN_EMA_TIME				—					IN2_EMA_EN		IN1_EMA_EN	
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12:8	IN_EMA_TIME	EMA filter time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0E = 16384 samples 0x0A = 1024 samples 0x0F = 32768 samples 0x0B = 2048 samples 0x10 = 65536 samples 0x0C = (Default) 4096 samples 0x11–0x1F = Reserved 0x0D = 8192 samples
7:2	—	Reserved
1	IN2_EMA_EN	Channel 2 EMA filter enable. 0 = (Default) Disabled 1 = Enabled
0	IN1_EMA_EN	Channel 1 EMA filter enable. 0 = (Default) Disabled 1 = Enabled

7.5.4 IN_PAD_CFG

Address: 0x0000 2140

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						IN2_PAD_LD_EN	IN1_PAD_LD_EN	—						IN2_PAD_AUTO_EN	IN1_PAD_AUTO_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	IN2_PAD_LD_EN	PAD level detector (LD) enable for Channel 2. 0 = (Default) Disabled 1 = Enabled
8	IN1_PAD_LD_EN	PAD level detector (LD) enable for Channel 1. 0 = (Default) Disabled 1 = Enabled
7:2	—	Reserved
1	IN2_PAD_AUTO_EN	Channel 2 PAD automatic response enable. 0 = (Default) Disabled 1 = Enabled
0	IN1_PAD_AUTO_EN	Channel 1 PAD automatic response enable. 0 = (Default) Disabled 1 = Enabled

7.5.5 IN_PAD_SIGNAL

Address: 0x0000 2142

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN_PAD_LD_AVG	—											IN_PAD_LD_TIME			
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description
15	IN_PAD_LD_AVG	Selects averaged or instantaneous input signal for PAD high-level threshold level detection (LD). 0 = (Default) Averaged signal 1 = Instantaneous signal
14:5	—	Reserved
4:0	IN_PAD_LD_TIME	PAD level-detect time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved

7.5.6 IN1_PAD_THR

Address: 0x0000 2146

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN1_PAD_LOW_THR				—				IN1_PAD_HIGH_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN1_PAD_LOW_THR	Channel 1 PAD level detector (LD) low-level threshold. 0x0–0x2 = Reserved 0x3 = –32 dBFS ... 0x9 = –68 dBFS 0xA = (Default) –74 dBFS 0xB–0xE = Reserved 0xF = mute
7:5	—	Reserved
4:0	IN1_PAD_HIGH_THR	Input Channel 1 PAD level detector (LD) high-level threshold. The listed threshold values apply to signal detection using the averaged signal level, the stated values represent the approximate signal levels that would be detected as above the threshold. If signal detection uses the instantaneous signal level the stated thresholds are approximately 4 dB lower, where 0x00 = –1 dBFS ... (step = –1 dBFS) ... 0x1F = –32 dBFS. 0x00–0x03 = Reserved 0x04 = –1 dBFS ... 0x09 = (Default) –6 dBFS ... 0x1F = –28 dBFS

7.5.7 IN2_PAD_THR
Address: 0x0000 214A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_PAD_LOW_THR				—				IN2_PAD_HIGH_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN2_PAD_LOW_THR	Channel 2 PAD level detector (LD) low-level threshold. 0x0–0x2 = Reserved 0x3 = –32 dBFS ... 0x9 = –68 dBFS 0xA = (Default) –74 dBFS 0xB–0xE = Reserved 0xF = mute
7:5	—	Reserved
4:0	IN2_PAD_HIGH_THR	Input Channel 2 PAD level detector (LD) high-level threshold. The listed threshold values apply to signal detection using the averaged signal level, the stated values represent the approximate signal levels that would be detected as above the threshold. If signal detection uses the instantaneous signal level the stated thresholds are approximately 4 dB lower, where 0x00 = –1 dBFS ... (step = –1 dBFS) ... 0x1F = –32 dBFS. 0x00–0x03 = Reserved 0x04 = –1 dBFS ... 0x09 = (Default) –6 dBFS ... 0x1F = –28 dBFS

7.5.8 IN_SIG_ACT_EN
Address: 0x0000 2170

RW	15...8	7	6	5	4	3	2	1	0
	—	—						IN_SIG_ACT_EN	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1:0	IN_SIG_ACT_EN	Input signal-activity detection enable. 00 = (Default) Disabled 01–10 = Reserved 11 = Enabled

7.5.9 IN1_SIG_ACT_THR
Address: 0x0000 2176

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN1_SIG_ACT_HIGH_THR				—				IN1_SIG_ACT_LOW_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN1_SIG_ACT_HIGH_THR	Channel 1 signal-activity detection, high-level threshold. 0x0–0x2 = Reserved 0x3 = –32 dBFS ... 0xA = (Default) –74 dBFS 0xB–0xE = Reserved 0xF = mute
7:4	—	Reserved
3:0	IN1_SIG_ACT_LOW_THR	Channel 1 signal-activity detection, low-level threshold. 0x0–0x2 = Reserved 0x3 = –74 dBFS ... 0x7 = (Default) –98 dBFS 0x8–0xE = Reserved 0xF = mute

7.5.10 IN2_SIG_ACT_THR
Address: 0x0000 217A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_SIG_ACT_HIGH_THR				—				IN2_SIG_ACT_LOW_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN2_SIG_ACT_HIGH_THR	Channel 2 signal-activity detection high-level threshold. 0x0–0x2 = Reserved 0x3 = –32 dBFS ... 0xA = (Default) –74 dBFS 0xB–0xE = Reserved 0xF = mute
7:4	—	Reserved
3:0	IN2_SIG_ACT_LOW_THR	Channel 2 signal-activity detection low-level threshold. 0x0–0x2 = Reserved 0x3 = –74 dBFS ... 0x7 = (Default) –98 dBFS 0x8–0xE = Reserved 0xF = mute

7.5.11 IN1_CFG_GPIO
Address: 0x0000 2202

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN1_GPI_POL	—	IN1_GPI_SEL			—				IN1_GPO4_SEL	IN1_GPO3_SEL	IN1_GPO2_SEL	IN1_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	IN1_GPI_POL	GPI polarity for Input Channel 1. 0 = (Default) GPI not inverted 1 = GPI inverted
11	—	Reserved
10:8	IN1_GPI_SEL	Select GPIO pin as GPI for Input Channel 1. 000 = (Default) Select GPI disabled 001 = Select GPIO1 010 = Select GPIO2 011 = Select GPIO3 100 = Select GPIO4 101–111 = Reserved
7:4	—	Reserved
3	IN1_GPO4_SEL	Input Channel 1 GPO4 configuration. 0 = (Default) Disabled 1 = Enabled
2	IN1_GPO3_SEL	Input Channel 1 GPO3 configuration. 0 = (Default) Disabled 1 = Enabled
1	IN1_GPO2_SEL	Input Channel 1 GPO2 configuration. 0 = (Default) Disabled 1 = Enabled
0	IN1_GPO1_SEL	Input Channel 1 GPO1 configuration. 0 = (Default) Disabled 1 = Enabled

7.5.12 IN2_CFG_GPIO
Address: 0x0000 2206

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN2_GPI_POL	—	IN2_GPI_SEL			—				IN2_GPO4_SEL	IN2_GPO3_SEL	IN2_GPO2_SEL	IN2_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	IN2_GPI_POL	GPI polarity for Input Channel 2. 0 = (Default) GPI not inverted 1 = GPI inverted

Bits	Name	Description
11	—	Reserved
10:8	IN2_GPI_SEL	Select GPIO pin as GPI for Input Channel 2. 000 = (Default) Select GPI disabled 001 = Select GPIO1 010 = Select GPIO2 011 = Select GPIO3 100 = Select GPIO4 101–111 = Reserved
7:4	—	Reserved
3	IN2_GPO4_SEL	Input Channel 2 GPO4 configuration 0 = (Default) Disabled 1 = Enabled
2	IN2_GPO3_SEL	Input Channel 2 GPO3 configuration 0 = (Default) Disabled 1 = Enabled
1	IN2_GPO2_SEL	Input Channel 2 GPO2 configuration. 0 = (Default) Disabled 1 = Enabled
0	IN2_GPO1_SEL	Input Channel 2 GPO1 configuration. 0 = (Default) Disabled 1 = Enabled

7.5.13 IN1_INT_GAIN

Address: 0x0000 222E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_UPDATE	—	IN1_INT_ANA_GAIN	—	IN1_INT_DIG_GAIN											
Access	WO	—	RW	—	RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_UPDATE	Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_INT_ANA_GAIN	Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN1_INT_DIG_GAIN	Channel 1 digital gain. Note the signal level is also controlled by the digital volume. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x0FF = 31.875 dB 0x100 = –32.000 dB 0x1FF = –0.125 dB

7.5.14 IN2_INT_GAIN

Address: 0x0000 222E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_UPDATE	—	IN2_INT_ANA_GAIN	—	IN2_INT_DIG_GAIN											
Access	WO	—	RW	—	RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_UPDATE	Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN2_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB

Bits	Name	Description
11:9	—	Reserved
8:0	IN2_INT_DIG_GAIN	Input Channel 2 digital gain. Note that the signal level is also controlled by the digital volume. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x0FF = 31.875 dB 0x100 = -32.000 dB 0x1FF = -0.125 dB

7.5.15 IN1_LOW_GPO

Address: 0x0000 2262

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_LOW_GPO4	IN1_LOW_GPO3	IN1_LOW_GPO2	IN1_LOW_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_LOW_GPO4	Channel 1 low gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN1_LOW_GPO3	Channel 1 low gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN1_LOW_GPO2	Channel 1 low gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN1_LOW_GPO1	Channel 1 low gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.5.16 IN1_LOW_INT_GAIN

Address: 0x0000 2266

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_LOW_UPDATE	—	IN1_LOW_INT_ANA_GAIN	—				IN1_LOW_INT_DIG_GAIN								
Access	WO	—	RW	—				RW								
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_LOW_UPDATE	Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_LOW_INT_ANA_GAIN	Input Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN1_LOW_INT_DIG_GAIN	Input Channel 1 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x0FF = 31.875 dB 0x100 = -32.000 dB 0x1FF = -0.125 dB

7.5.17 IN2_LOW_GPO
Address: 0x0000 226A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_LOW_GPO4	IN2_LOW_GPO3	IN2_LOW_GPO2	IN2_LOW_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_LOW_GPO4	Channel 2 low gain GPO4 logic output 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN2_LOW_GPO3	Channel 2 low gain GPO3 logic output 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN2_LOW_GPO2	Channel 2 low gain GPO2 logic output 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN2_LOW_GPO1	Channel 2 low gain GPO1 logic output 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.5.18 IN2_LOW_INT_GAIN
Address: 0x0000 226E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_LOW_UPDATE	—	IN2_LOW_INT_ANA_GAIN	—	IN2_LOW_INT_DIG_GAIN											
Access	WO	—	RW	—	RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_LOW_UPDATE	Input Channel 2 gain update. Write 1 to apply Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN2_LOW_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN2_LOW_INT_DIG_GAIN	Input Channel 2 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x0FF = 31.875 dB 0x100 = -32.000 dB ... 0x1FF = -0.125 dB

7.5.19 IN1_HIGH_GPO
Address: 0x0000 22C2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_HIGH_GPO4	IN1_HIGH_GPO3	IN1_HIGH_GPO2	IN1_HIGH_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_HIGH_GPO4	Channel 1 high gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN1_HIGH_GPO3	Channel 1 high gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN1_HIGH_GPO2	Channel 1 high gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high

Bits	Name	Description
12	IN1_HIGH_GPO1	Channel 1 high gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.5.20 IN1_HIGH_INT_GAIN

Address: 0x0000 22C6

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_HIGH_UPDATE	—	IN1_HIGH_INT_ANA_GAIN	—	IN1_HIGH_INT_DIG_GAIN											
Access	WO	—	RW	—	RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_HIGH_UPDATE	Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_HIGH_INT_ANA_GAIN	Input Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN1_HIGH_INT_DIG_GAIN	Input Channel 1 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x0FF = 31.875 dB 0x100 = -32.000 dB 0x1FF = -0.125 dB

7.5.21 IN2_HIGH_GPO

Address: 0x0000 22CA

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_HIGH_GPO4	IN2_HIGH_GPO3	IN2_HIGH_GPO2	IN2_HIGH_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_HIGH_GPO4	Channel 2 high gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN2_HIGH_GPO3	Channel 2 high gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN2_HIGH_GPO2	Channel 2 high gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN2_HIGH_GPO1	Channel 2 high gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.5.22 IN2_HIGH_INT_GAIN

Address: 0x0000 22CE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_HIGH_UPDATE	—	IN2_HIGH_INT_ANA_GAIN	—	IN2_HIGH_INT_DIG_GAIN											
Access	WO	—	RW	—	RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_HIGH_UPDATE	Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved

Bits	Name	Description
13:12	IN2_HIGH_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN2_HIGH_INT_DIG_GAIN	Input Channel 2 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB ... 0x1FF = -0.125 dB 0x0FF = 31.875 dB

7.5.23 OUT_SIG_ACT_EN

Address: 0x0000 2510

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12:8	OUT_EMA_TIME	Signal activity detection level-detect EMA filter time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved
7:2	—	Reserved
1:0	OUT_SIG_ACT_EN	Output signal activity detection enable. 00 = (Default) Disabled 01–10 = Reserved 11 = Enabled

7.5.24 OUT1_SIG_ACT_THR

Address: 0x0000 2514

RW	15...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—
Default	0x00	0	0	0	0	1	0	0	1

Bits	Name	Description
15:5	—	Reserved
4:0	OUT1_SIG_ACT_THR	Signal activity detection level-detect threshold. 0x00–0x02 = Reserved 0x03 = -2 dBFS ... 0x09 = (Default) -38 dBFS 0x13 = -98 dBFS 0x14–0x1F = Reserved

7.5.25 OUT2_SIG_ACT_THR

Address: 0x0000 2518

RW	15...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—
Default	0x00	0	0	0	0	1	0	0	1

Bits	Name	Description
15:5	—	Reserved
4:0	OUT2_SIG_ACT_THR	Signal activity detection level-detect threshold. 0x00–0x02 = Reserved 0x03 = -2 dBFS ... 0x09 = (Default) -38 dBFS 0x13 = -98 dBFS 0x14–0x1F = Reserved

7.6 PIN_CONFIG

7.6.1 PAD_IRQ_CFG

Address: 0x0000 3D1C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ_OP_CFG	—						GPIO1_IRQ_EN	GPIO2_IRQ_EN	—		CONFIG4_IRQ_EN	SPI_SCK_IRQ_EN	—		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IRQ_OP_CFG	IRQ output configuration 0 = (Default) CMOS 1 = Open drain
14:9	—	Reserved
8	GPIO1_IRQ_EN	IRQ output to GPIO1 0 = (Default) GPIO1 1 = IRQ output
7	GPIO2_IRQ_EN	IRQ output to GPIO2 0 = (Default) GPIO2 1 = IRQ output
6:5	—	Reserved
4	CONFIG4_IRQ_EN	CONFIG4 pin function select 0 = (Default) HW config/CH_IDLE 1 = IRQ output
3	SPI_SCK_IRQ_EN	IRQ output to SPI_SCK 0 = (Default) SPI_SCK 1 = IRQ output
2:0	—	Reserved

7.7 IRQ_CONFIG

7.7.1 IRQ_STS

Address: 0x0000 3E04

RO	15...8	7	6	5	4	3	2	1	0
	—	—						IRQ_STS	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IRQ_STS	IRQ status. Logical OR of all unmasked x_INT interrupts. 0 = (Default) Not asserted 1 = Asserted

7.7.2 IRQ_ADC_EVENT_INT

Address: 0x0000 3E1C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_PAD_LOW_INT	IN1_PAD_LOW_INT	IN2_PAD_HIGH_INT	IN1_PAD_HIGH_INT	GAIN_CONFLICT_INT	—			IN2_CLIP_WARN_INT	IN1_CLIP_WARN_INT	—	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11	IN2_PAD_LOW_INT	ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceeds Low Th
10	IN1_PAD_LOW_INT	ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceeds Low Th
9	IN2_PAD_HIGH_INT	ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th

Bits	Name	Description
8	IN1_PAD_HIGH_INT	ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th
7	GAIN_CONFLICT_INT	Gain updates both high gain and low gain concurrently interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Update conflict
6:3	—	Reserved
2	IN2_CLIP_WARN_INT	Channel 2 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
1	IN1_CLIP_WARN_INT	Channel 1 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
0	—	Reserved

7.7.3 IRQ_ADC_EVENT_MASK

Address: 0x0000 3E2C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—				IN2_PAD_LOW_MASK	IN1_PAD_LOW_MASK	IN2_PAD_HIGH_MASK	IN1_PAD_HIGH_MASK	GAIN_CONFLICT_MASK	—					IN2_CLIP_WARN_MASK	IN1_CLIP_WARN_MASK	—
Default	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	

Bits	Name	Description
15:12	—	Reserved
11	IN2_PAD_LOW_MASK	ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
10	IN1_PAD_LOW_MASK	ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
9	IN2_PAD_HIGH_MASK	ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
8	IN1_PAD_HIGH_MASK	ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
7	GAIN_CONFLICT_MASK	Gain updates both high gain and low gain interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
6:3	—	Reserved
2	IN2_CLIP_WARN_MASK	ADC Channel 2 clip-detect warning interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
1	IN1_CLIP_WARN_MASK	ADC Channel 1 clip-detect warning interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
0	—	Reserved

7.7.4 IRQ_ADC_EVENT_STS
Address: 0x0000 3E5C

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_PAD_LOW_STS	IN1_PAD_LOW_STS	IN2_PAD_HIGH_STS	IN1_PAD_HIGH_STS	—					IN2_CLIP_WARN_STS	IN1_CLIP_WARN_STS	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11	IN2_PAD_LOW_STS	ADC Channel 2 PAD LD, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted
10	IN1_PAD_LOW_STS	ADC Channel 1 PAD LD, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted
9	IN2_PAD_HIGH_STS	ADC Channel 2 PAD LD, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
8	IN1_PAD_HIGH_STS	ADC Channel 1 PAD LD, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
7:3	—	Reserved
2	IN2_CLIP_WARN_STS	ADC Channel 2 clip warning status. 0 = (Default) Not asserted 1 = Asserted
1	IN1_CLIP_WARN_STS	ADC Channel 1 clip warning status. 0 = (Default) Not asserted 1 = Asserted
0	—	Reserved

8 Thermal Characteristic

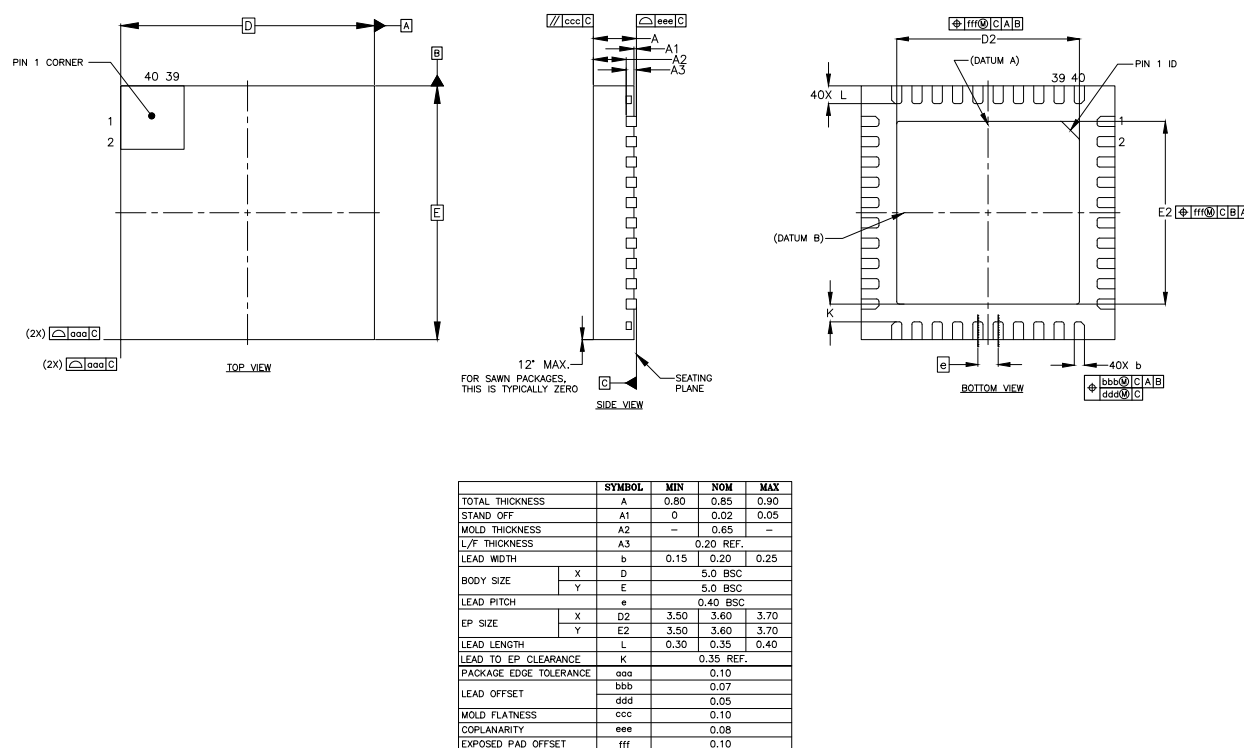
Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	30.25	°C/W
Junction-to-board thermal resistance	θ_{JB}	17.17	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	69.26	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	15.99	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	2.82	°C/W

Notes:

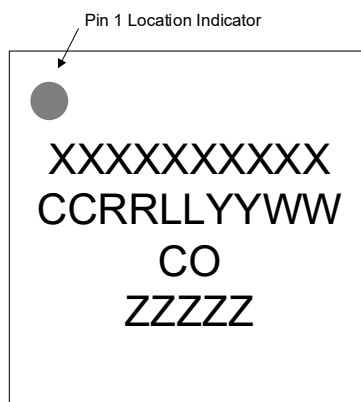
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

9 Package Dimensions


Figure 9-1. QFN Package Drawing

10 Package Marking

Figure 10-1. Package Marking



Top Side Brand

Line 1: Part number
 Line 2: Package mark
 Line 3: Country of origin (CO)
 Line 4: Encoded wafer/device ID

Package Mark Fields

CC = Cirrus Logic Index Code
 RR = Device revision code
 LL = Lot sequence code
 YY = Year of manufacture
 WW = Work week of manufacture

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	Environmental Certifications	Grade	Temperature Range	Container	Orderable Part Number
CS4233B	High Performance Two-Channel Audio Codec	40-pin QFN	RoHS Compliant	Commercial	-40 to +85°C	Tray	CS4233B-DN
						Tape and Reel	CS4233B-DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, <https://www.nxp.com>

13 Revision History

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Table 13-1. Revision History

Revision	Change
A3 OCT 2026	- Updated Dynamic Range and THD+N values in Specifications. - Updated Pin Assignments and Descriptions (changes reflected throughout) (Section 1): - Renamed Pin 1 was GND_D, now NC; PAD was GND_A, now GND. - Changed LDO_VD_FILT power supply, was VDD_A1 now VDD_A2. - Updated table note related to ground connections - Updated Typical Connections Diagram (Section 2): - Renamed GND_D, GND_A, and PAD, as summarized above. - Updated decoupling capacitor values on ADC_FILT_x and LDO_VD_FILT pins. - Updated note regarding clocking option configuration. - Added External Component Requirements (Table 2-1). - Updated Characteristics and Specifications (Section 3): - Updated bandwidth condition for performance measurements in Parameter Definitions table note (Table 3-1) - Removed GND_D from test conditions in all tables (Section 3). - Updated table note for Recommended Operating Conditions (Table 3-2). - Added Digital Core (LDO_VD_FILT) to Absolute Maximum Ratings (Table 3-3). - Updated Dynamic Range (A-weighted) and THD_N (0 dBFS) values and table notes in ADC Path Characteristics (Table 3-4). - Added load to test conditions and updated THD_N and Load Resistance parameters in DAC Path Characteristics (Table 3-5). - Updated parameter conditions for Passband ripple and Stopband attenuation for Slow roll-off filter at $F_S = 352.8$ kHz or 384 kHz in ADC Filter Characteristics (Table 3-6) - Removed Phase Deviation specification in ADC High Pass Filter Characteristics (Table 3-7). - Updated Passband ripple parameter conditions for Balanced roll-off filter at $F_S = 352.8$ kHz or 384 kHz in DAC Filter Characteristics (Table 3-8). - Removed Phase deviation specification in DAC High Pass Filter Characteristics (Table 3-9). - Update test conditions and parameters in Device Power Consumption (Table 3-10). - Removed table note regarding XTAL pin multiplexing in Digital Interface Specifications and Characteristics (Table 3-11). - Removed note related to DAC_FILT maximum output current in DC Characteristics (Table 3-12). - Removed specification and related note for ADC_FILT maximum output current in DC Characteristics (Table 3-12). - Updated VDD_IO2 POR threshold (V_{POR}) rising and falling maximum values in DC Characteristics (Table 3-12). - Removed reference to half-cycle mode in ASP timing in I2S and Left-Justified Modes parameter note in Switching Specifications—Audio Serial Port (ASP) (Table 3-14). - Updated VDD_IO in test conditions in Switching Specifications—SPI Control Port (Table 3-16).

Table 13-1. Revision History (Cont.)

Revision	Change
A3 OCT 2026	- Updated Functional Description (Section 4): —Clarified supported sample rates for different system clock frequencies (Section 4.2, Section 4.4, Section 4.4.1, Section 4.4.2, Section 4.8.1, Section 4.8.3). —Clarified external clock synchronization requirements in ASP Secondary Mode (Section 4.4.1, Section 4.4.2, Section 4.8.1). —Corrected debounce time and input polarity configuration availability in Virtual PAD (Section 4.5.5). —Added note in Automatic PAD Response (Section 4.5.5.3). —Corrected operation ADC input path, including removal of Idle detection in Signal-Activity Detection (Section 4.7).—Added signal-activity detection capability on DAC output path in Signal-Activity Detection (Section 4.7). —Updated IRQ Event Logic Output Pins and removed signal-activity detection status in Interrupts (Section 4.10). - Updated Applications (Section 5): —Updated attenuation level for -12 dB/octave slope in Input Buffer Circuit (Section 5.1) —Updated diagrams and associated equations Output Buffer Circuit (Section 5.2). —Added PCB Layout Guidelines (Section 5.3). - Edited Registers (Section 7): —MTLREVID —INx_PAD_LOW_THR —INx_PAD_HIGH_THR —IN_SIG_ACT_HIGH/LOW_EN —INx_SIG_ACT_HIGH/LOW_THR —OUTx_GPI_POL —OUTx_DIG_GAIN —INx_SIG_ACT_LOW/HIGH_INT —INx_SIG_ACT_LOW/HIGH_MASK —INx_SIG_ACT_LOW/HIGH_STS —IN_SIG_ACT_LD_TIME —INx_EMA_EN —OUT_SIG_ACT_EN —OUTx_SIG_ACT_THR —OUT_EMA_TIME_
A2 MAY 2026	Released for public distribution
A1 NOV 2025	Initial version

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

IMPORTANT NOTICE

"Advance" product information describes products that are in development and subject to substantial development changes. For the purposes of our terms and conditions of sale, "Preliminary" or "Advanced" datasheets are nonfinal datasheets that include, but are not limited to, datasheets marked as "Target", "Advance", "Product Preview", "Preliminary Technical Data" and/or "Preproduction." Products provided with any such datasheet are therefore subject to relevant terms and conditions associated with "Preliminary" or "Advanced" designations, as set out in our terms and conditions of sale, including but not limited to that Cirrus Logic expressly disclaims any warranties with respect to such products. The products and services of Cirrus Logic International (UK) Limited; Cirrus Logic, Inc.; and other companies in the Cirrus Logic group (collectively either "Cirrus Logic" or "Cirrus") are sold subject to Cirrus Logic's terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. Software is provided pursuant to applicable license terms. Cirrus Logic reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Cirrus Logic to verify that the information is current and complete. Testing and other quality control techniques are utilized to the extent Cirrus Logic deems necessary. Specific testing of all parameters of each device is not necessarily performed. In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Cirrus Logic is not liable for applications assistance or customer product design. The customer is solely responsible for its overall product design, end-use applications, and system security, including the specific manner in which it uses Cirrus Logic components. Certain uses or product designs may require an intellectual property license from a third party. Features and operations described herein are for illustrative purposes only and do not constitute a suggestion or instruction to adopt a particular product design or a particular mode of operation for a Cirrus Logic component.

CIRRUS LOGIC PRODUCTS ARE NOT DESIGNED, TESTED, INTENDED OR WARRANTED FOR USE (1) WITH OR IN IMPLANTABLE PRODUCTS OR FDA/ MHRA CLASS III (OR EQUIVALENT CLASSIFICATION) MEDICAL DEVICES, OR (2) IN ANY PRODUCTS, APPLICATIONS OR SYSTEMS, INCLUDING WITHOUT LIMITATION LIFE-CRITICAL MEDICAL EQUIPMENT OR SAFETY OR SECURITY EQUIPMENT, WHERE MALFUNCTION OF THE PRODUCT COULD CAUSE PERSONAL INJURY, DEATH, SEVERE PROPERTY DAMAGE OR SEVERE ENVIRONMENTAL HARM. INCLUSION OF CIRRUS LOGIC PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS LOGIC DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS LOGIC PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS LOGIC PRODUCTS IN SUCH A MANNER, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS LOGIC, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

This document is the property of Cirrus Logic, and you may not use this document in connection with any legal analysis concerning Cirrus Logic products described herein. No license to any technology or intellectual property right of Cirrus Logic or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property rights. Any provision or publication of any third party's products or services does not constitute Cirrus Logic's approval, license, warranty or endorsement thereof. Cirrus Logic gives consent for copies to be made of the information contained herein only for use within your organization with respect to Cirrus Logic integrated circuits or other products of Cirrus Logic, and only if the reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices and conditions (including this notice). This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. This document and its information is provided "AS IS" without warranty of any kind (express or implied). All statutory warranties and conditions are excluded to the fullest extent possible. No responsibility is assumed by Cirrus Logic for the use of information herein, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. Cirrus Logic, Cirrus, the Cirrus Logic logo design, and SoundClear are among the trademarks of Cirrus Logic. Other brand and product names may be trademarks or service marks of their respective owners.

Copyright © 2025–2026 Cirrus Logic, Inc. and Cirrus Logic International Semiconductor Ltd. All rights reserved.

SPI is a trademark of Motorola.